User Manual

BMP561

Arm® Cortex®-M0+ Core-based 32-bit MCU

Version: V1.0

Contents

1 Introduction and Document Description Rules

1.1 Introduction

BMP561 is a gauge chip, with the core based on Arm® Cortex®-M0+, and the system bus is based on the AHB-Lite advanced high-performance bus protocol. It can achieve fast processing and storage of data in combination with high-speed memory. The peripheral bus is based on the APB advanced peripheral bus protocol and can be used to expand rich peripherals, ensuring fast and flexible connection.

For information about Arm® Cortex®-M0+ core, refer to *Technical Reference Manual of Arm® Cortex®-M0+*. For model information, dimensions and electrical characteristics of components, refer to the corresponding datasheet.

We hereby declare that: Zhuhai Geehy Semiconductor Co., Ltd. is hereinafter referred to as "Geehy".

2 System Architecture

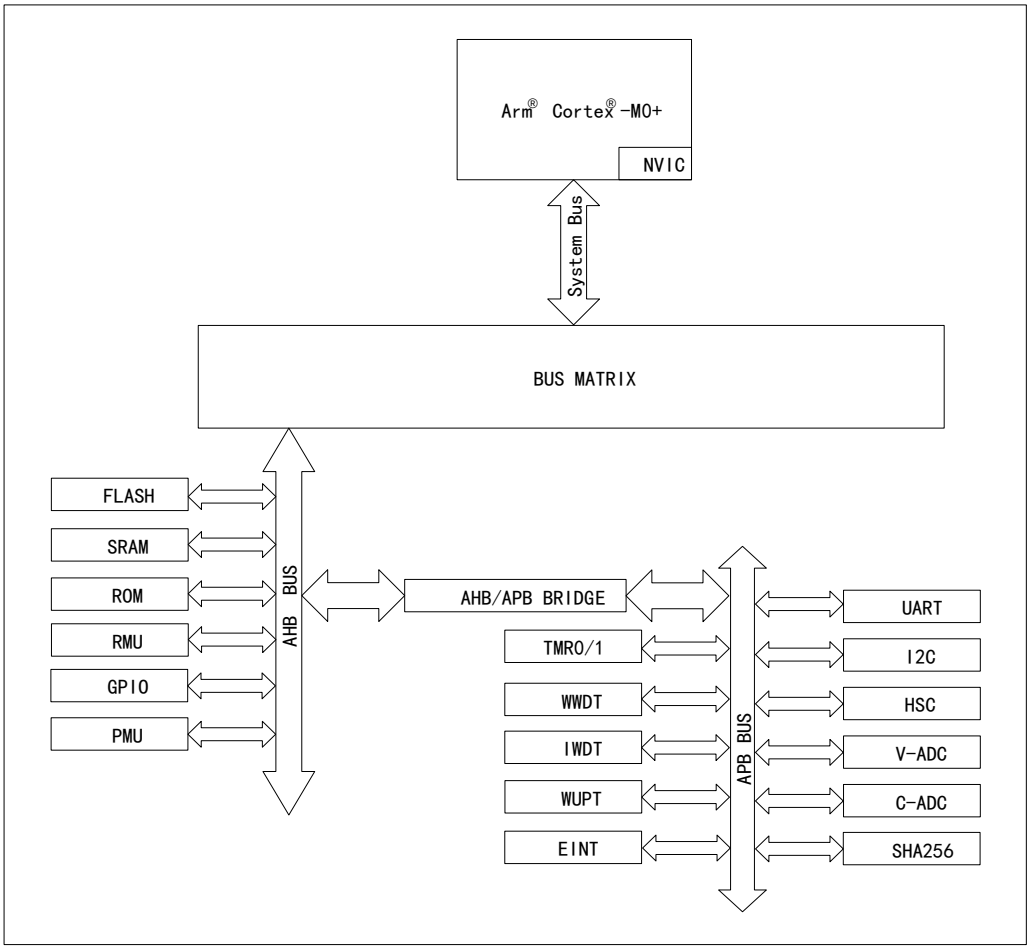
2.1 Full Name and Abbreviation Description of Terms

Table 1 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Advanced High-Performance Bus	AHB
Advanced Peripheral Bus	APB

2.2 System architecture block diagram

Figure 1 System Architecture Block Diagram



3 System Control (SYSCTRL)

3.1 Full Name and Abbreviation Description of Terms

Table 2 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
System Control	SYSCTRL

3.2 Introduction

The system control module includes power management, clock management, reset management, and other system related control. For detailed information, refer to the corresponding chapter of each module.

3.3 Register address mapping

Table 3 SYSCTRL Register Address Mapping

Register name	Description	Offset address
SYSCTRL_KEY	Unlock register	0x00
SYSCTRL_SCCR	Master clock control register	0x04
SYSCTRL_AHBBCG	AHB clock gating register	0x08
SYSCTRL_APBBCG	APB peripheral bus clock gating register	0x0C
SYSCTRL_APBWCG	APB peripheral work clock gating register	0x10
SYSCTRL_AHBRSTCR	AHB peripheral reset control register	0x14
SYSCTRL_APBRSTCR	APB peripheral reset control register	0x18
SYSCTRL_RSTSR	System reset source state register	0x1C
SYSCTRL_LPMCR	System low-power mode register	0x20
SYSCTRL_LPCR	System low-power configuration register	0x24
SYSCTRL_STA	System communication start bit detection register	0x28
SYSCTRL_WUSR	System wake-up flag register	0x2C
SYSCTRL_RSTSRCLR	System reset source state clear register	0x30
SYSCTRL_STACLR	System communication start bit detection flag clear register	0x34
SYSCTRL_WUSRCLR	System wake-up flag clear register	0x38
SYSCTRL_HSICLKCR	HSI clock control register	0x3C
SYSCTRL_LSICLKCR	LSI clock control register	0x40
SYSCTRL_ANACR	System analog peripheral control register	0x44

Register name	Description	Offset address
SYSCTRL_DEBUGCR	System debug control register	0x48
SYSCTRL_BOOTCR	System BOOT control register	0x4C

3.4 Register functional description

3.4.1 Unlock register (SYSCTRL_KEY)

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	LOCKKEY	W	Lock Key Password protection configuration for system register write operation: 1. Before operating on the SYSCTRL system register, it must be unlocked by writing 0x87E4 to the Key value. 2. After unlocking the system register, the KEYST0 flag bit will be set, and writing 1 to this bit will lock it.
16	KEYST	W	Key Status After unlocking the system register, the KEYST flag bit will be set, and writing 1 to this bit will lock it. Note: Writing 0 is invalid, and writing 1 will lock it.
31:17	Reserved		

3.4.2 Master clock control register (SYSCTRL_SCCR)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
2:0	SYSCLKDIV	R/W	SYSCLK Division 0: 1 frequency division (no frequency division) 1: 2 frequency division … N: 2^N frequency division
3	SYSCLKSEL	R/W	SYSCLK Select 0: Select HSICLK 1: Select LSICLK
5:4	APBCLKDIV	R/W	HSICLK Division 0: 1 frequency division (no frequency division) 1: 2 frequency division 2: 4 frequency division 3: 8 frequency division Note: The default value is to be determined
6	SWBUSY	R	Switch Busy 0: In progress of clock switching or no clock switching 1: In progress of clock switching
31:7	Reserved		

3.4.3 AHB clock gating register (SYSCTRL_AHBBCG)

Offset address: 0x08

Reset value: 0x0000 000F

Field	Name	R/W	Description
0	FLSBCEN	R/W	FLASH Bus Clock Enable 0: Disable 1: Enable
1	GPIOBCEN	R/W	GPIO Bus Clock Enable 0: Disable 1: Enable
2	AHB2APBCEN	R/W	AHB to APB Clock Enable 0: Disable 1: Enable
3	ROMBCEN	R/W	ROM Bus Clock Enable 0: Disable 1: Enable
31:4	Reserved		

3.4.4 APB peripheral bus clock gating register (SYSCTRL_APBBCG)

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	WWDTBCEN	R/W	WWDT Bus Clock Enable 0: Disable 1: Enable
1	I2CBCEN	R/W	I2C Bus Clock Enable 0: Disable 1: Enable
2	HSCBCEN	R/W	HSC Bus Clock Enable 0: Disable 1: Enable
3	TMR0BCEN	R/W	TMR0 Bus Clock Enable 0: Disable 1: Enable
4	TMR1BCEN	R/W	TMR1 Bus Clock Enable 0: Disable 1: Enable
5	ADC0BCEN	R/W	C-ADC Bus Clock Enable 0: Disable 1: Enable
6	ADC1BCEN	R/W	V-ADC Bus Clock Enable 0: Disable 1: Enable
7	Reserved		
8	UARTBCEN	R/W	UART Bus Clock Enable

Field	Name	R/W	Description
			0: Disable 1: Enable
9	SHABCEN	R/W	SHA Bus Clock Enable 0: Disable 1: Enable
10	IWDTBCEN	R/W	IWDT Bus Clock Enable 0: Disable 1: Enable
11	WUPTBCEN	R/W	WUPT Bus Clock Enable 0: Disable 1: Enable
12	EINTBCEN	R/W	EINT Bus Clock Enable 0: Disable 1: Enable
31:13	Reserved		

Note: When accessing the module register, it is necessary to ensure that the corresponding work clock of the module has been enabled; otherwise, some registers of some modules not to be able to be written to.

3.4.5 APB peripheral work clock gating register (SYSCTRL_APBWCG)

Offset address: 0x10

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	WWDTWCEN	R/W	WWDT Work Clock Enable 0: Disable 1: Enable
1	I2CWCEN	R/W	I2C2 Work Clock Enable 0: Disable 1: Enable
2	HSCWCEN	R/W	HSC Work Clock Enable 0: Disable 1: Enable
3	TMR0WCEN	R/W	TMR0 Work Clock Enable 0: Disable 1: Enable
4	TMR1WCEN	R/W	TMR1 Work Clock Enable 0: Disable 1: Enable
5	ADC0WCEN	R/W	C-ADC Work Clock Enable 0: Disable 1: Enable
6	ADC1WCEN	R/W	V-ADC Work Clock Enable 0: Disable 1: Enable

Field	Name	R/W	Description
7	Reserved		
8	UARTWCEN	R/W	UART Work Clock Enable 0: Disable 1: Enable
9	SHAWCEN	R/W	SHA Work Clock Enable 0: Disable 1: Enable
10	IWDTWCEN	R/W	IWDT Work Clock Enable 0: Disable 1: Enable
11	WUPTWCEN	R/W	WUPT Work Clock Enable 0: Disable 1: Enable
12	EINTWCEN	R/W	EINT Work Clock Enable 0: Disable 1: Enable
31:13	Reserved		

3.4.6 AHB peripheral reset control register (SYSCTRL_AHBRSTCR)

Offset address: 0x14

Reset value: 0x0000 0003

Field	Name	R/W	Description
0	FLSRST	R/W	FLASH Reset 0: Reset 1: Release
1	GPIORST	R/W	GPIO Reset 0: Reset 1: Release
31:2	Reserved		

3.4.7 APB peripheral reset control register (SYSCTRL_APBRSTCR)

Offset address: 0x18

Reset value: 0x0000 1FFF

Field	Name	R/W	Description
0	WWDTRST	R/W	WWDT Reset 0: Reset 1: Release
1	I2CRST	R/W	I2C Reset 0: Reset 1: Release
2	HSCRST	R/W	HSC Reset 0: Reset 1: Release

Field	Name	R/W	Description
3	TMR0RST	R/W	TMR0 Reset 0: Reset 1: Release
4	TMR1RST	R/W	TMR1 Reset 0: Disable 1: Enable
5	ADC0RST	R/W	C-ADC Reset 0: Reset 1: Release
6	ADC1RST	R/W	V-ADC Reset 0: Reset 1: Release
7	Reserved		
8	UARTRST	R/W	UART Reset 0: Reset 1: Release
9	SHARST	R/W	SHA Reset 0: Reset 1: Release
10	IWDTRST	R/W	IWDT Reset 0: Reset 1: Release
11	WUPTRST	R/W	WUPT Reset 0: Reset 1: Release
12	EINTRST	R/W	EINT Reset 0: Reset 1: Release
31:13	Reserved		

3.4.8 System reset source status register (SYSCTRL_RSTSR)

Offset address: 0x1C

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	WWDTRSR	R	WWDT Reset Source Flag 0: No IWDT reset generated 1: IWDT reset generated
1	IWDTRSR	R	IWDT Reset Source Flag 0: No IWDT reset generated 1: IWDT reset generated
2	SYSRSR	R	SYSRSR Reset Source Flag 0: No SYSRSTREQ reset generated 1: SYSRSTREQ reset generated
3	OPLRSR	R	Option-bytes Reset Source Flag

Field	Name	R/W	Description
			0: No option byte load reset generated 1: Option byte load reset generated
4	LPRSR	R	Low Power Reset Source Flag 0: No Hibernate low-power reset generated 1: Hibernate low-power reset generated
5	PORRSR	R	POR Reset Source Flag 0: No power-on/power-down reset occurs 1: Power-on/power-down reset occurs
31:6	Reserved		

3.4.9 System low-power mode register (SYSCTRL_LPMCR)

Offset address: 0x20

Reset value: 0x0000 0000

Field	Name	R/W	Description
1:0	LPM	R/W	Low Power Mode 00: WAIT status 01: SLEEP status 10: DPSLEEP status 11: HIBERNATE status
31:2	Reserved		

Note: This register will only reset during power-on reset, and the watchdog reset will be unaffected.

3.4.10 System low-power configuration register (SYSCTRL_LPCR)

Offset address: 0x24

Reset value: 0x0000 00FD

Field	Name	R/W	Description
0	LDO_LP	R/W	LDO Low Power 1: Enable 0: Disable
1	HSI_LPSEL	R/W	HSI Low Power Select When entering the DPSLEEP state, select the HSI status 1: Enter the ultra-low power state, with a frequency of approximately 700kHz 0: Sub-low power mode, with a frequency of approximately 1.4MHz
7:2	WAITLDO	R/W	Wait LDO When LDO_LP is enabled and it exits from the SLEEP or DPSLEEP state, it will wait for WAITLDO SYS_CK until LDO becomes stable. 0:1 clock cycle 1: 2 clock cycles ..... N: N+1 clock cycles
8	LPE	R/W	Low Power Enable

Field	Name	R/W	Description
			Used for control of low-power state entry. 1 can only be written to LPE when LPCR_KEY is equal to 0xA5A5. When the system exits the low-power mode, the system will automatically clear this bit to 0. 1: Enable entering the low-power mode 0: Disable
15:9	Reserved		
31:16	LPCR_KEY	R/W	Low Power Key When LPCR_KEY is equal to 0xA5A5, LPE can be written.

3.4.11 System communication start bit detection register (SYSCTRL_STA)

Offset address: 0x28

Reset value: 0x0000 0008

Field	Name	R/W	Description
0	STA_WUPEN	R/W	Start Wake-up Enable This bit is determined based on the system configuration COMM_MODE. 1: Enable 0: Disable Note: Only when the PMU enters the HIBERNATE and DPSLEEP status, will the I2C start bit or HSC-BREAK be detected, and the hardware will pull down the SCL and SDA pins; refer to STA_AUTO Settings for details.
1	STA_ AUTO	R/W	Start Auto When the system enters DPSLEEP status, if STA_WUPEN is enabled, STA_AUTO will be configured to 1, and the hardware will pull down the SCL and SDA pins (when COMM is 1, pull down SCL; when COMM is 0, only pull down SDA) until the software writes 1 to STA_WUPFCLR and the I2C bus will be released. Otherwise, when STA_ AUTO is configured to 0, after PMU exits the DPSLEEP status (i.e. the CPU is running instructions or the system is exiting the reset), the system will release the bus. When the system enters DPSLEEP status, if STA_WUPEN is enabled, STA_ AUTO will be configured to 0, and the hardware will pull down the SCL and SDA pins (when COMM is 1, pull down SCL; when COMM is 0, only pull down SDA) until PMU exits Hibernate mode (i.e. CPU is running instructions or the system is exiting reset), the system will release the bus, and Hibernate mode STA_AUTO will be set to 1 as an invalid value. 1: Manual mode 0: Automatic mode
2	STA_WUPIE	R/W	Start Wake-up Interrupt Enable 1: Enable 0: Disable
3	COMM_MODE	R/W	Communication Mode

Field	Name	R/W	Description
			1: Select I2C mode 0: Select HSC mode
4	STA_FLAG	R/W	Start Flag The value of 1 indicates the I2C start bit or HSC-BREAK is detected, and writing 1 to this bit can clear STA_FLAG.
31:5	Reserved		

Note: This function will be used before entering DPSLEEP or HIBERNATE status. To prevent conflicts between STA detection and I2C/HSC module, STA detection is disabled in other scenarios.

3.4.12 System wake-up flag register (SYSCTRL_WUSR)

Offset address: 0x2C

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	I2C_WUF	R	I2C Wake-Up Flag 0: No I2C/HSC interrupt wake-up 1: I2C/HSC interrupt wake-up occurs
1	HSC_WUF	R	HSC Wake-Up Flag 0: No I2C/HSC interrupt wake-up 1: I2C/HSC interrupt wake-up occurs
2	UART_WUF	R	UART Wake-Up Flag 0: No UART interrupt wake-up 1: UART interrupt wake-up occurs
3	IWDT_WUF	R	IWDT Wake-Up Flag 0: No wake-up event occurs 1: Wake-up event occurs
4	Reserved		
5	TMR0_WUF	R	TMR0 Wake-Up Flag 0: No TMR0 interrupt wake-up 1: TMR0 interrupt wake-up occurs
6	TMR1_WUF	R	TMR1 Wake-Up Flag 0: No TMR1 interrupt wake-up 1: TMR1 interrupt wake-up occurs
7	ADC0_WUF	R	C-ADC Wake-Up Flag 0: No C-ADC interrupt wake-up 1: C-ADC interrupt wake-up occurs
8	ADC1_WUF	R	V-ADC Wake-Up Flag 0: No ADC interrupt wake-up 1: ADC interrupt wake-up occurs
9	FLASH_WUF	R	FLASH Wake-Up Flag 0: No FLASH interrupt wake-up 1: FLASH interrupt wake-up occurs
10	WUPT_WUF	R	WUPT Wake-Up Flag 0: No WUPT event wake-up 1: WUPT event wake-up occurs

Field	Name	R/W	Description
11	STA_WUF	R	I2C/HSC Wake-Up Flag 0: No I2C/HSC start bit event wake-up occurs 1: I2C/HSC start bit event wake-up occurs
12	EINT0_WUF	R	EINT0 Wake-Up Flag 0: No EINT0 interrupt wake-up 1: EINT0 interrupt wake-up occurs
13	EINT1_WUF	R	EINT1 Wake-Up Flag 0: No EINT1 interrupt wake-up 1: EINT1 interrupt wake-up occurs
14	EINT2_WUF	R	EINT2 Wake-Up Flag 0: No EINT2 interrupt wake-up 1: EINT2 interrupt wake-up occurs
15	SHA256_WUF	R	SHA256 Wake-Up Flag 0: No SHA256 interrupt wake-up 1: SHA256 interrupt wake-up occurs
31:16	Reserved		

3.4.13 System reset source status clear register (SYSCTRL_RSTSRCLR)

Offset address: 0x30

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	WWDTRSRCLR	W	WWDT Reset Source Flag Clear Write 1 to this bit to clear it to 0.
1	IWDTRSRCLR	W	IWDT Reset Source Flag Clear Write 1 to this bit to clear it to 0.
2	SYSRSRCLR	W	System Reset Source Flag Clear Write 1 to this bit to clear it to 0.
3	OPLRSRCLR	W	Option-bytes Reset Source Flag Clear Write 1 to this bit to clear it to 0.
4	LPRSRCLR	W	Low Power Reset Source Flag Clear Write 1 to this bit to clear it to 0.
5	PORRSRCLR	W	POR Reset Source Flag Clear Write 1 to this bit to clear it to 0.
31:6	Reserved		

3.4.14 System communication start bit detection flag clear register (SYSCTRL_STACLR)

Offset address: 0x34

Reset value: 0x0000 0000

Field	Name	R/W	Description
3:0	Reserved		
4	STA_FLAGCLR	W	Start Flag Clear

Field	Name	R/W	Description
			Write 1 to this bit to clear it to 0.
31:5	Reserved		

3.4.15 System wakeup flag clear register (SYSCTRL_WUSRCLR)

Offset address: 0x38

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	I2C_WUFCLR	W	I2C Wake-up Clear Write 1 to this bit to clear it to 0.
1	HSC_WUFCLR	W	HSC Wake-up Clear Write 1 to this bit to clear it to 0.
2	UART_WUFCLR	W	UART Wake-up Clear Write 1 to this bit to clear it to 0.
3	IWDT_WUFCLR	W	IWDT Wake-up Clear Write 1 to this bit to clear it to 0.
4	Reserved		
5	TMR0_WUFCLR	W	TMR0 Wake-up Clear Write 1 to this bit to clear it to 0.
6	TMR1_WUFCLR	W	TRM1 Wake-up Clear Write 1 to this bit to clear it to 0.
7	ADC0_WUFCLR	W	C-ADC Wake-up Clear Write 1 to this bit to clear it to 0.
8	ADC1_WUFCLR	W	V-ADC Wake-up Clear Write 1 to this bit to clear it to 0.
9	FLASH_WUFCLR	W	FLASH Wake-up Clear Write 1 to this bit to clear it to 0.
10	WUPT_WUFCLR	W	WUPT Wake-up Clear Write 1 to this bit to clear it to 0.
11	STA_WUFCLR	W	STA Wake-up Clear Write 1 to this bit to clear it to 0.
12	EINT0_WUFCLR	W	EINT0 Wake-up Clear Write 1 to this bit to clear it to 0.
13	EINT1_WUFCLR	W	EINT1 Wake-up Clear Write 1 to this bit to clear it to 0.
14	EINT2_WUFCLR	W	EINT2 Wake-up Clear Write 1 to this bit to clear it to 0.
15	SHA256_WUFCLR	W	SHA256 Wake-up Clear Write 1 to this bit to clear it to 0.
31:16	Reserved		

3.4.16 HSI clock control register (SYSCTRL_HSICLKCR)

Offset address: 0x3C

Reset value: 0x0000 0020

Field	Name	R/W	Description
2:0	Reserved		
4:3	HSICLKDIV	R/W	HSICLK Division 0: 1 frequency division (no frequency division) 1: 2 frequency division 2: 4 frequency division 3: 8 frequency division Note: The default value is to be determined.
5	HSICLKRDY	R	HSICLK Ready This bit is set to 1 or cleared to 0 by hardware. 0: HSICLK is not ready 1: HSICLK is ready
31:6	Reserved		

3.4.17 LSI clock control register (SYSCTRL_LSICLKCR)

Offset address: 0x40

Reset value: 0x0000 0003

Field	Name	R/W	Description
0	LSICLKEN	R/W	LSICLK Enable This bit is set to 1 and cleared to 0 by software, and is set to 1 by hardware in the following situations: When SYSCLKSEL selects LSICLK as the master clock or PMU enters DPSLEEP status. 0: Turn off the internal high-speed clock 1: Turn on the internal high-speed clock
1	LSICLKRDY	R	LSICLK Ready This bit is set to 1 or cleared to 0 by hardware. 0: LSICLK is not ready 1: LSICLK is ready
31:2	Reserved		

3.4.18 System analog peripheral control register (SYSCTRL_ANACR)

Offset address: 0x44

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	NTCRPUEN	R/W	NTC Pull-up Resistor Enable 1: Enable 0: Disable
1	TSEN	R/W	TS Enable 1: Enable 0: Disable
7:2	Reserved		
9:8	LVDISEL	R/W	LVD Select 00: 0.08uA 01: 0.72uA

Field	Name	R/W	Description
			10: 5uA 11: 45uA
13:10	SYSLVDVSEL	R/W	System LVD Select 0000: 1.8V 0001: 1.9V 0010: 2.0V 0011：2.1 V 0100：2.2V 0101: 2.3V 0110: 2.4V 0111: 2.5V 1000: 2.6V 1001: 2.7V 1010: 2.8V 1011: 2.9V 1100: 3.0V 1101: 3.1V 1110: 3.2V 1111: 3.3V
14	SYSLVDEN	R/W	System LVD Enable Note: The LVDEN of Option Byte can also enable LVD. When SYSLVDEN is 1, SYSLVDVSEL controls the detection threshold of LVD.
15	Reserved		
18:16	VADCMUXSEL	R/W	V-ADC MUX Select 000：mux_bat_5p0 001：mux_bat_sns_5p0 010：mux_ntc_5p0 011：mux_ipat_5p0 (internal ts output) 100：mux_vss_5p0 101：dvdd1p5 110: Reserved 111: Reserved
20:19	Reserved		
21	AFECLKEN	R/W	AFE Clock Enable Enable the AFE clock required for C-ADC and V-ADC. 0: Disable 1: Enable
22	AFEEN	R/W	AFE Enable Enable AFE required for C-ADC/ADC/NTC. 0: Disable 1: Enable
31:23	Reserved		

3.4.19 System debug control register (SYSCTRL_DEBUGCR)

Offset address: 0x48

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	SYSDEBUGEN	R/W	System Debug Enable 0: Disable 1: Enable
3:1	SYSDEBUGSEL	R/W	System Debug Select 000: HSIDIV_CLK clock (clock obtained after HSICLK undergoes HSIDIV frequency division) 001: LSI clock Others: Reserved
4	PAD23FILSEL	R/W	Pad 2 and Pad 3 Filter Select When it is 1, PAD2 and PAD3 pass through a 100ns filter circuit and are then sent to GPIO/I2C.
31:5	Reserved		

3.4.20 System BOOT control register (SYSCTRL_BOOTCR)

Offset address: 0x4C

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	REMAPSEL	R/W	Remap Select 1: Select SYSREMAP[1:0] as the remapping control 0: Select boot1~0 of Option Byte as the remapping control
2:1	SYSREMAP	R/W	System Remap When REMAPSEL is 1, SYSREMAP controls the mapping region. 00: System 0 address is mapped to FLASH space 01: System 0 address is mapped to ROM space 10: System 0 address is mapped to RAM space 11: System 0 address is mapped to ROM space
31:3	Reserved		

4 Flash Memory (FLASH)

4.1 Full Name and Abbreviation Description of Terms

Table 4 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Flash Memory	FLASH
Data Flash	DFLASH
Sector	SEC
Non-Volatile RAM	NVR
Read Out Protection	RDP

4.2 Introduction

This chapter mainly introduces the storage structure, read, erase, write, read/write protection, unlock/lock characteristics of FLASH, and the involved register functional description.

4.3 Main characteristics

(1) 64KB on-chip flash memory for storing instructions and data

(2) 4KB of Data Flash space with write protection function

(3) Support 32-bit data read and write access

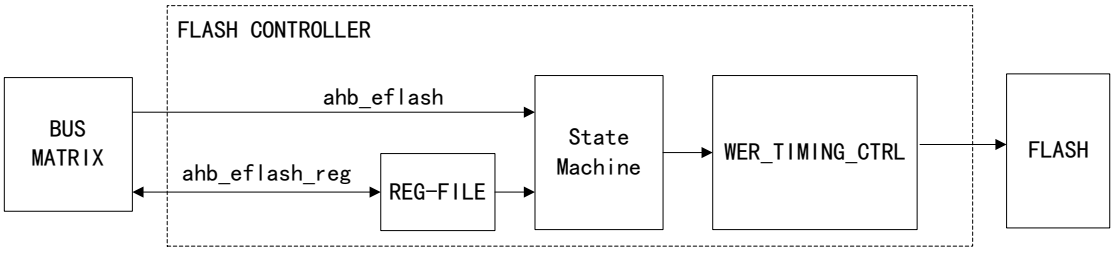
(4) Support low-power mode

(5) Equipped with security protection function to prevent illegal access to codes or data

(6) The minimum erase unit is 1 sector (512 bytes), and the minimum programming unit is 32 bits

4.4 Structure block diagram

Figure 2 Structure Block Diagram



4.5 Functional description

4.5.1 FLASH tasks

(1) Read and write protection processing for FLASH.

(2) Achieve reading and writing of data between MCU and FLASH.

(3) Perform sector erase and chip erase on Flash.
- The main array sector supports sector/chip erase.
- NVR sector only supports sector erase.

(4) Automatically load initialization information after power on, and after reset, the hardware automatically loads option byte information to FLASH.

4.5.2 FLASH modules

(1) reg_file: Complete the register configuration of the module.

(2) state_machine: Complete the data flow control, low power consumption, read and write protection management, and erase timing control of the entire functional module.

(3) wer_timing_ctrl: Complete erase timing control.

4.5.3 Low-power state

FLASH provides Deep Standby mode to reduce power consumption. After the LPM and WFE instructions are set by software, the hardware automatically controls the clock of FLASH through REQ/ACK handshake.

The wake-up source causes the system to exit the low-power state, and FLASH will also automatically exit the low-power state.

4.5.4 Regional functional partitioning

Figure 3 Functional Partitioning of FLASH Regions

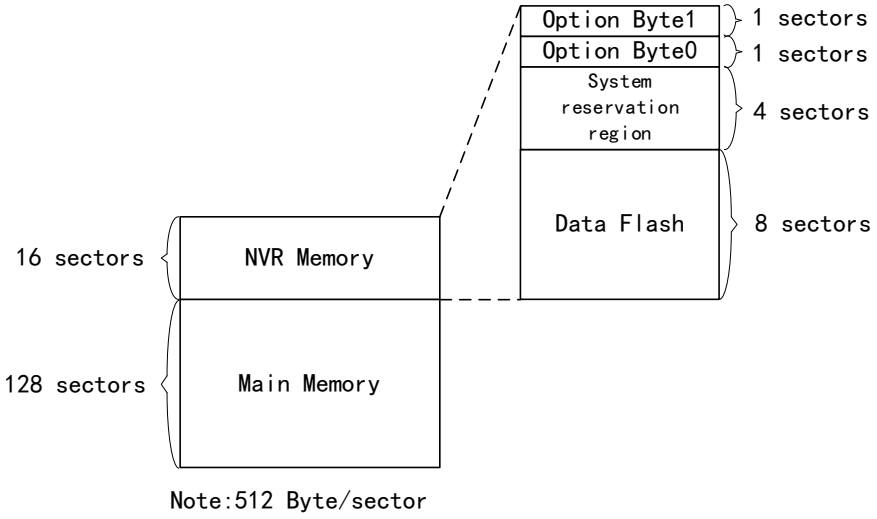


Table 5 FLASH Regions and Purposes

Zone	Size	Purpose
Main Flash	128x512=64KB	Main storage region, used for storing codes
Data Flash	8x512=4KB	Used by users, examples as storing user key, authentication Key, and some program configurations.
System reservation region	4x512=2KB	System reservation
Option Byte0	512 B	RDP code protection (occupying only one word of the sector) 1. RDP[7:0] Level0: 0xAA, without protection Level1: Values other than 0xCC and 0xAA; the debugging interface cannot access the internal RAM or FLASH program region and Data Flash region. Level2: 0xCC; disable the debugging port, and disable BOOT from RAM region. Option Byte0 can only be erased and programmed through the SWD debugging interface. When attempting to modify RDP to level0 under level1 conditions, the Flash program region will be erased. If the DFP for the corresponding Data Flash space is configured to 1b'1, this region will also be erased.
Option Byte1	512 B	Data Flash protection, watchdog enable, FLASH write protection lock. Data Flash Protection (DFP); when the RDP protection level changes from level1 to level0, the hardware automatically erases the Main region, and Data Flash can be optionally erased (decide

Zone	Size	Purpose
		which sectors need to be erased depending on the DFP configuration). 1. DFP[7:0] DFP[0]=0x0: When SWD modifies RDP to be unencrypted, this sector will not be erased. DFP[0]=0x1: When SWD modifies RDP to be unencrypted, this sector will be erased. DFP[7:1] corresponds to the Data Flash space of each sector. 2. IWDTEN/WWDTEN, which is watchdog enable 3. FLASH Main region write protection lock The FLASH program region is logically divided into 32 banks, each with a size of 4 sectors, or 2K, and each bank space can be independently equipped with erase protection function. 0x33: Disable WLOCK Others: Enable WLOCK WLOCK[31:0] is write protection enable bit: 0: The sector write protection of this region is enabled 1: The sector write protection of this region is disabled 4. LVDEN and LVDVSEL selection When RDP is at level1, DFP cannot modify the configuration value from 1 to 0. For example, when DFP[0] is 1, it cannot be modified to 0 in the protection state of level1; if Option Byte1 does not satisfy the requirements for positive and inverse code check, FLASH_OBR[DFP] will be forced to 0xFF.

4.5.5 FLASH protection

Table 6 Flash Protection

Zone	RDP protection level	User code execution			Debugging, SRAM startup		
		Read	Write	Erase	Read	Write	Erase
Main Flash/Data Flash	0	Y	Y	Y	Y	Y	Y
	1	Y	Y	Y	N	N	N
	2	Y	Y	Y	F	F	F
Option Bytes 1	0	Y	Y	Y	Y	Y	Y
	1	Y	Y	Y	Y	Y	Y
	2	Y	Y	Y	F	F	F
Option Bytes 0	0	Y	N	N	Y	Y[1]	N
	1	Y	N	N	Y	Y[1]	N
	2	Y	N	N	F	F	F

Note:

(1) Read Protection (RDP) can only be modified through the SWD interface. When the encryption level is changed from encryption 1 to encryption 0, Main Flash and Data Flash will be automatically erased (configured as DFP[7:0]; whether erasing the corresponding sector of Data Flash is optional).

(2) When level2 protection is enabled, the debugging port and boot from RAM are disabled.

(3) The debugging interfaces at level1 cannot read and write SRAM.

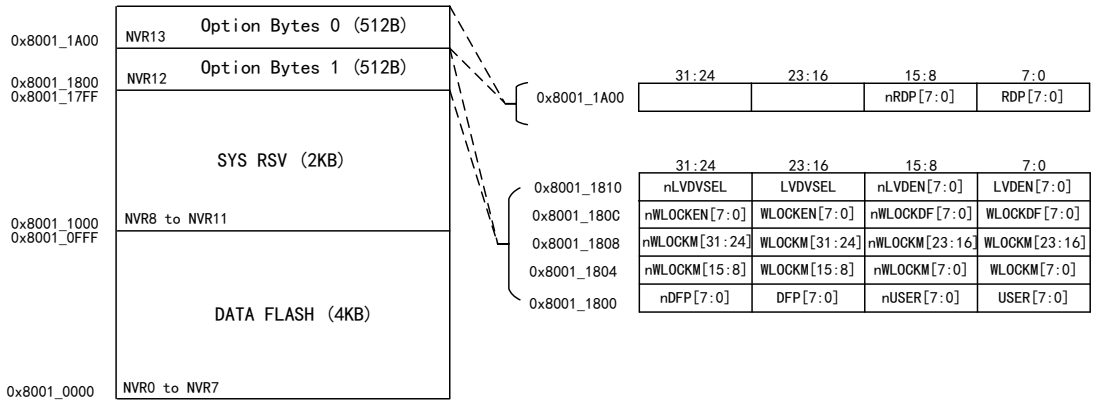
(4) When RDP is changed to be unprotected (from level1 to level0), the Main Flash will be erased.

(5) The system region is the only readable region in any situation.

(6) All option bytes except RDP bytes can be reprogrammed.

4.5.6 Storage content settings

Figure 4 Storage Content Settings



4.5.7 FLASH unlock

FLASH requires Key verification before erasing, and each Key has a sequential write detection state machine. When the write sequence is wrong or the write value is wrong, or when erasing or programming is performed before the FLASH_KEY/FLASH_OPTKEY register is verified correctly, the FLASH operation will enter an error state and generate corresponding interrupt. After the Key authentication error occurs to FLASH, erasing FLASH will be disabled until the next reset. However, after normal erasing is completed, writing any value to the FLASH_KEY register will restore the state machine to its initial write protection state.

Note: The same Key can only unlock one region at a time. For example, when the user needs to write Data Flash again after finishing writing Main Flash, first restore the FLASH_KEY register to the write protection state, and then unlock the Data Flash. Similarly, it is the same for the FLASH_OPTKEY register.

Table 7 Flash Unlock Collection

Register	Key	Main Flash	Data Flash (NVR0~NVR7)	Option Bytes0 (NVR13)	Option Bytes1 (NVR12)
FLASH_KEY	Key1	0x9696 9696	0xF3E2 D1C0	-	-

Register	Key	Main Flash	Data Flash (NVR0~NVR7)	Option Bytes0 (NVR13)	Option Bytes1 (NVR12)
	Key2	0x3C3C 3C3C	0x01FE 2C3D	-	-
FLASH_OPTKEY	Key1	-	-	0xAAAA BBBB	0xCCCC DDDD
	Key2	-	-	0x4455 6677	0x5566 7788

4.5.8 FLASH erase

Table 8 Flash Unlock Collection

Main Flash	Data Flash （NVR0~NVR7）	Option Bytes1 (NVR12)	Option Bytes0 (NVR13)
Chip/Sector	Sector	Sector	-

4.5.8.1 Chip erase

This operation is specifically for erasing the chip, and the steps are as follows:

(1) Check FLASH_SR[BUSY] bit to confirm that the last programming operation has completed.

(2) Write the unlock sequence to the FLASH_KEY register to unlock the Main Flash area.

(3) Detect FLASH_SR[KEYSTA].

(4) Set FLASH_CR[ERTYPE] to 0x10 (Chip Erase).

(5) Set FLASH_CR[EREQ] bit to 1.

(6) Write 0xA5A5 to any address in the Main Flash area.

(7) Set FLASH_SR[BUSY] bit to zero.

(8) The MCU reads all pages and verifies.

4.5.8.2 Main Flash erase

This operation is specifically for erasing the Main Flash, and the steps are as follows:

(1) Check FLASH_SR[BUSY] bit to confirm that the last programming operation has completed.

(2) Write the unlock sequence to the FLASH_KEY register to unlock the Main Flash area.

(3) Detect FLASH_SR[KEYSTA].

(4) Set FLASH_CR[ERTYPE] to 0x01 (Main Erase).

(5) Set FLASH_CR[EREQ] bit to 1.

(6) Write 0xA5A5 to any address in the Main Flash area.

(7) Set FLASH_SR[BUSY] bit to zero.

(8) The MCU reads all pages and verifies.

4.5.8.3 Sector erase

Sector erase is not supported for Option Bytes 0 (NVR13).

Sector Erase for Option Bytes 1 (NVR12)

(1) Check FLASH_SR[BUSY] bit to confirm that the last programming operation has completed.

(2) Write the unlock sequence to the FLASH_OPTKEY register to unlock the Option Bytes 1 area.

(3) Detect FLASH_SR[KEYSTA].

(4) Set FLASH_CR[ERTYPE] to 0x00 (Sector Erase).

(5) Set FLASH_CR[EREQ] bit to 1.

(6) Write 0xA5A5 to any address in the Option Bytes area.

(7) Set FLASH_SR[BUSY] bit to zero.

(8) The MCU reads all pages and verifies.

Sector Erase for Other Areas

(1) Check FLASH_SR[BUSY] bit to confirm that the last programming operation has completed.

(2) Write the unlock sequence to the FLASH_KEY register to unlock the corresponding area.

(3) Detect FLASH_SR[KEYSTA].

(4) Set FLASH_CR[ETYPE] to 0x00 (Sector Erase).

(5) Set FLASH_CR[EREQ] bit to 1.

(6) Write 0xA5A5 to any address in the corresponding FLASH area.

(7) Set FLASH_SR[BUSY] bit to zero.

(8) The MCU reads all pages and verifies.

4.5.9 FLASH programming

4.5.9.1 Programming Option Bytes 0 (SWD Only)

(1) Check FLASH_SR[BUSY] bit to confirm that the last programming operation has completed.

(2) Write the unlock sequence to the FLASH_OPTKEY register to unlock the Option Bytes 0 (NVR13) area.

(3) Detect FLASH_SR[OPTKEYSTA].

(4) Set FLASH_CR[PREQ] bit to 1.

(5) Write data (word) to the target address.

(6) Hardware automatically erases the NVR13 area.

(7) Wait for FLASH_SR[BUSY] bit to set to zero.

(8) The MCU reads the data at that address and verifies.

(9) Either power cycle the device or write 1 to FLASH_CR[FORCE_OPTLOAD] to update the RDP state.

4.5.9.2 Programming Option Bytes 1

(1) Check FLASH_SR[BUSY] bit to confirm that the last programming operation has completed.

(2) Write the unlock sequence to the FLASH_OPTKEY register to unlock the Option Bytes 1 (NVR12) area.

(3) Detect FLASH_SR[OPTKEYSTA].

(4) Set FLASH_CR[PREQ] bit to 1.

(5) Write data (word) to the target address.

(6) Wait for FLASH_SR[BUSY] bit to set to zero.

(7) The MCU reads the data at that address and verifies.

4.5.9.3 Programming Other Areas

(1) Check FLASH_SR[BUSY] bit to confirm that the last programming operation has completed.

(2) Write the unlock sequence to the FLASH_KEY register to unlock the Main Flash area.

(3) Detect FLASH_SR[KEYSTA].

(4) Set FLASH_CR[PREQ] bit to 1.

(5) Write data (word) to the target address.

(6) Wait for FLASH_SR[BUSY] bit to set to zero.

(7) The MCU reads the data at that address and verifies.

4.6 Register address mapping

Table 9 Flash Register Address Mapping

Register name	Description	Offset address
FLASH_KEY	Unlock the keyword register of FLASH	0x00
FLASH_OPTKEY	Unlock the option keyword register	0x04
FLASH_SR	Status register	0x08
FLASH_CR	Control register	0x0C
FLASH_TMCTRL	Time base control register	0x10
FLASH_OBR	Option byte register	0x14
FLASH_WLOCKDF	Write protection register of Data Flash region	0x18
FLASH_WLOCKM	Write protection register of Main region	0x1C

4.7 Register functional description

4.7.1 Unlock FLASH keyword register (FLASH_KEY)

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	FKEY	W	Flash Key Flash erases the key input register, and the software or SWD must correctly write a valid key sequence to this address before starting erase.

4.7.2 Unlock option keyword register (FLASH_OPTKEY)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	OPTKEY	W	Option Key It is used to enter keywords to unlock Option Bytes0 and Bytes1.

4.7.3 Status register (FLASH_SR)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	ERD	R	Erase Done Set by hardware reset, and write 1 by software to clear to 0
1	PRD	R	Program Done Set by hardware reset, and write 1 by software to clear to 0
2	BUSY	R	Flash Busy
3	KEYERR	R	Flash Key Error Set by hardware reset, and write 1 by software to clear to 0

Field	Name	R/W	Description
4	WRPRTERR	R	Write Protection Error This bit is applicable to Main Flash and Data Flash. When a write operation occurs to the write protected region, it is set by hardware. Write 1 and it can be cleared to 0. When ERRIE is enabled, an interrupt will be generated.
5	WADRERR	R	Write Address Error When writing data to the destination address during erasing or programming, an error will occur, and erasing or programming will not take effect. An error will occur in any of the following situations: 1. If the target region unlocked by the Key or the unlocked region does not match the actual written region, it will be automatically set to 1 by hardware, and can be cleared to 0 by software by writing 0 to it. 2. The target address is Option Byte0, and PREQ is not set to 1. 3. SWD attempts to modify the non-option_byte region (non-chip erase operation) when RDP is at level 1. 4. The user program attempts to modify Option Byte0. 5. The user program attempts to erase the chip. 6. During the erase operation, the last data written to the target address is not 0xA5A5.
16	TRIMERR	R	Trim Error In the process of TRIMLOAD, there is a positive and inverse code verification error in the trim information, and it is automatically set to 1 by hardware.
19:17	KEYSTA	R	Flash Key Status 000: Flash write protection status, with the Key not entered 011: Unlock the Main region 100: Unlock the Data Flash region 111: Key error locked status, which can only be unlocked after reset Others: Only one key is written
22:20	OPTKEYSTA	R	Flash Key Status 000: Write protection status, the Key not entered 010: Unlock the Option Byte0 region 100: Unlock the Option Byte1 region 111: Key error locked status, which can only be unlocked after reset Others: Only one key is written
31:23	Reserved		

4.7.4 Control register (FLASH_CR)

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	EREQ	R/W	Erase Request It is set by software, and can be automatically cleared to zero after the hardware completes erasing Note: When both EREQ and PREQ are set to 1, the hardware considers it as an EREQ request
1	PREQ	R/W	Program Request It is set by software, and can be automatically cleared to zero after the hardware completes programming Note: When both EREQ and PREQ are set to 1, the hardware considers it as an EREQ request
3:2	ERTYPE	R/W	Erase Type 00: Sector Erase 01: Main Erase 1x: Chip Erase (SWD only) Note: The difference between Chip Erase and Main Erase is that Chip Erase can erase the Data flash according to the DFP settings; when SR[BUSY] is at a high level, this register cannot be written.
4	EOPIE	R/W	Erase or Program Interrupt Enable When PRD or ERD is set to 1, it indicates the end of programming or erasing
5	ERRIE	R/W	Error interrupt Enable All error conditions including WADRERR, WRPRTERR, and KEYERR.
14:6	Reserved		
15	FORCE_OPTLOAD	R/W	Force Option Load This bit can only be written as 1 when the data written in the higher 16 bits at the same time is 0xA5A5. When written as 1, this bit will force the option byte to reload, and this operation will trigger a system reset. 0: Invalid 1: Valid
31:16	Reserved		

4.7.5 Time base control register (FLASH_TMCTRL)

Offset address: 0x10

Reset value: 0x0000 001F

Field	Name	R/W	Description
4:0	UNIT	R/W	Flash 1us Unit Counter FLASH erase time base control (subtracting 1 configuration), with 4MHz as the reference, 1us requires 4 Cycles, subtracting 1 configuration sets UNIT to 0x03; in actual use, it can be adjusted according to the Flash clock frequency (the clock cannot be lower than 1MHz in FLASH erase state)
31:5	Reserved		

4.7.6 Option byte register (FLASH_OBR)

Offset address: 0x14

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	OPTERR	R	Option Error When this bit is set, it indicates that the complementary relationship between RDP&NRDP, user&nuser, DFP and WLOCK fields is not established in loading option bytes.
1	LEVEL1_PROT	R	Level1 Protection When this bit is set, it indicates that it is currently in Level1 protection status (reset value=1)
2	LEVEL2_PROT	R	Level2 Protection When this bit is set, it indicates that it is currently in Level2 protection status
3	Reserved		
4	NBOOT0	R	nBoot0 When the user fields are full FF or are not complementary, this bit is 1
5	NBOOT1	R	nBoot1 When the user fields are full FF or are not complementary, this bit is 0
6	WWDTSW	R	WWDT Switch 0: Hardware activation 1: Software activation When the user fields are full FF or are not complementary, this bit is 1
7	IWDTSW	R	IWDT Switch 0: Hardware activation 1: Software activation When the user fields are full FF or are not complementary, this bit is 1
15:8	DFP	R	Data Flash Protection DFP[0]=0x0: When SWD modifies RDP to be unencrypted, this sector will not be erased DFP[0]=0x1: When SWD modifies RDP to be unencrypted, this sector will be erased DFP[7:1] corresponds to the Data Flash space of each sector
16	WLOCKEN	R	Write Lock Enable 1: Enable WLOCK 0: Disable WLOCK
17	LVDEN	R	Low Voltage Detection Enable Note: The LVDEN of Option Byte can also enable LVD. When SYSLVDEN, SYSLVDVSEL controls the detection threshold of LVD.
21:18	LVDVSEL	R	Low Voltage Detection Select 0000: 1.8V 0001: 1.9V 0010: 2.0V 0011: 2.1V 0100：2.2V

Field	Name	R/W	Description
			0101: 2.3V 0110: 2.4V 0111: 2.5V 1000: 2.6V 1001: 2.7V 1010: 2.8V 1011: 2.9V 1100: 3.0V 1101: 3.1V 1110: 3.2V 1111: 3.3V
31:22	Reserved		

4.7.7 Data Flash region write protection register (FLASH_WLOCKDF)

Offset address: 0x18

Reset value: 0x0000 00FF

Field	Name	R/W	Description
7:0	WLOCKDF	R	Write Lock Data Flash This register contains the write protection status loaded from the option byte. Each sector of Data Flash corresponds to 1bit WRPDF. Data Flash has a total of 8 sectors, counting from 0. DFWRP[0]=0, indicating that the 0 sector of the first Data Flash is write-protected and cannot be programmed or erased. DFWRP[0]=1, indicating that the 0 sector of the first Data Flash is non-write-protected and can be programmed and erased.
31:8	Reserved		

4.7.8 Main region write protection register (FLASH_WLOCKM)

Offset address: 0x1C

Reset value: 0xFFFF FFFF

Field	Name	R/W	Description
31:0	WLOCKM	R	Write Lock Main Flash This register contains the write protection status loaded from the option byte. Every four sectors of Main Flash correspond to 1bit WRP. Main Flash has a total of 128 sectors, counting from 0. WRP[0]=0, indicating that the 0 sector of the first Main Flash is write-protected. It cannot be programmed or erased. WRP[0]=1, indicating that the 0 sector of the first Main Flash is non-write-protected. It can be programmed and erased.

5 Clock Management Unit (CMU)

5.1 Full Name and Abbreviation Description of Terms

Table 10 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
High Speed Internal Clock	HSICLK
Low Speed Internal Clock	LSICLK
Low Power Oscillator	LPO
System Clock Generator	SCG
System Oscillator	SYSOSC

5.2 Introduction

The chip uses two different clock sources to drive the system. The clock inside the chip integrates these clock sources to generate the clocks required for the operation of each module.

5.3 Clock source

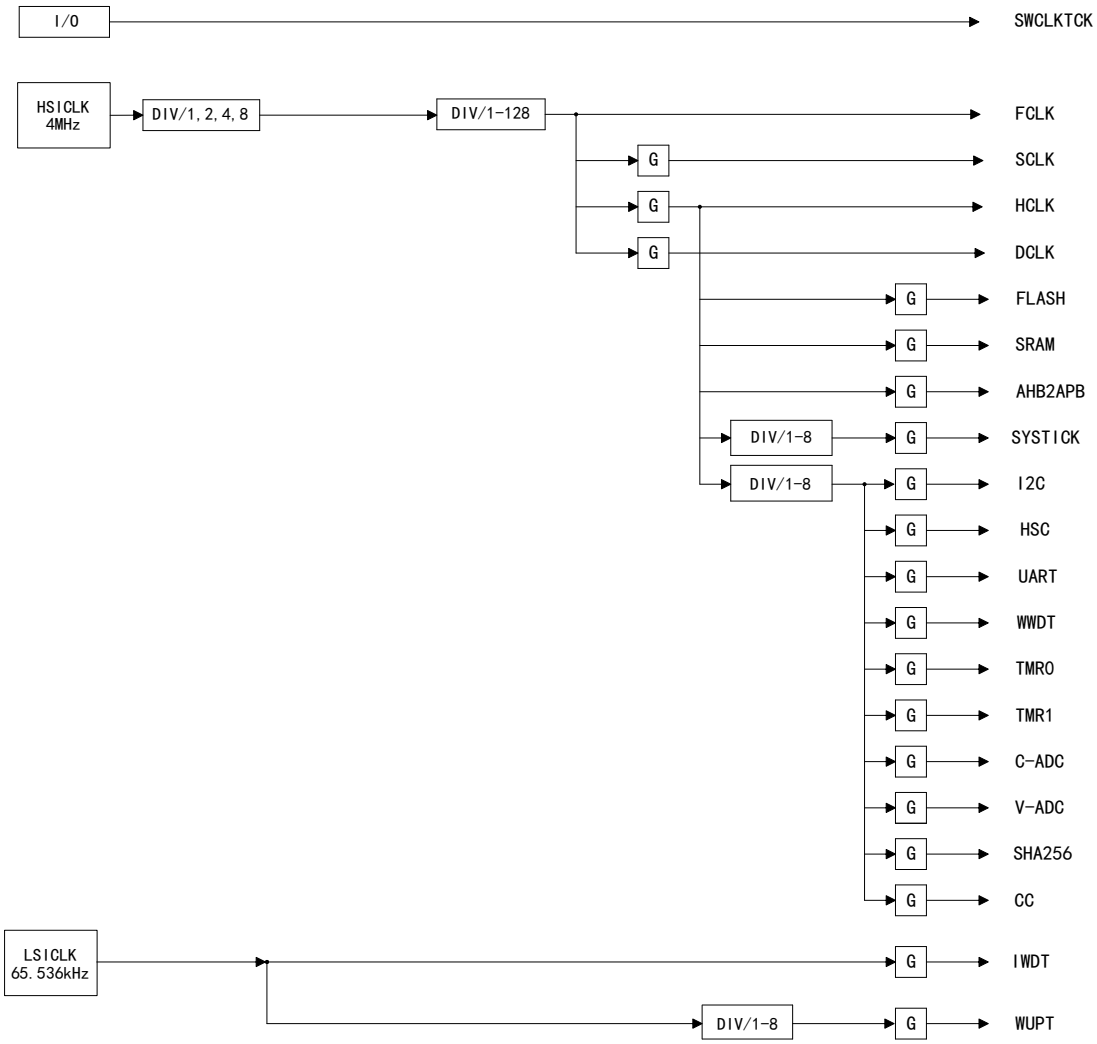
(1) Two different clock sources are supported:
- HSICLK oscillator clock, 4MHz internal RC oscillator
- LSICLK oscillator clock, 65.536kHz internal RC oscillator

(2) Provide a bus clock and work clock that can be separately turned off by software for all modules in the chip.

(3) Support even frequency division of the main clock HSICLK.

5.4 Clock tree

Figure 5 Clock Tree



Note: G represents gating, used to turn off and on the clock.

5.5 Clock enable and master clock switching

5.5.1 HSICLK enable

(1) HSICLK is fixed to be enabled, namely HSICLK cannot be turned off by software.

(2) When entering the DPSLEEP state, the PMU can configure whether to turn off HSICLK or make it operate in a low-power state.

5.5.2 LSICLK enable

After LSICLK and HSICLK are turned on again, the count needs to reach a certain value before the clock can output. The user can query whether HSICLK or LSICLK is ready by reading the status bit of

SYSCTRL_HSICLKCR[HSICLKRDY] or SYSCTRL_LSICLKCR[LSICLKRDY].

5.6 Register address mapping

Related registers:

- SYSCTRL_SCCR
- SYSCTRL_AHBBCG
- SYSCTRL_APBBCG
- SYSCTRL_APBWCG
- SYSCTRL_HSICLKCR
- SYSCTRL_LSICLKCR

Refer to Register Address Mapping in "System Control (SYSCTRL)".

5.7 Register functional description

Refer to Register Function Description in "System Control (SYSCTRL)".

6 Nested Vector Interrupt Controller (NVIC)

6.1 Full Name and Abbreviation Description of Terms

Table 11 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Non Maskable Interrupt	NMI
Nested Vectored Interrupt Controller	NVIC

6.2 Introduction

The Arm® Cortex®-M0+ core of the chip integrates NVIC, which is tightly coupled with the core, and can implement exception and interrupt processing and power management control efficiently and with low latency.

6.3 Main characteristics

(1) 23 maskable interrupt channels (excluding 16 Arm® Cortex®-M0+ interrupt lines) and 4 priorities.

(2) The tightly coupled NVIC interface can directly pass interrupt vector entry addresses to the core, and achieve low-latency interrupt response.

(3) Give priority to processing of high-priority interrupts, able to automatically save the processor state, and automatically recover when the interrupt returns, without additional instructions.

(4) This module provides flexible interrupt management function with minimal interrupt latency.

6.4 Interrupt vector table

Table 12 Interrupt Vector Table

Priority	Priority type	Name	Description	Address
-	-	-	MSP initial value	0x0000_0000
-3	Fixed	Reset	Reset	0x0000_0004
-2	Fixed	NMI	Non-maskable interrupt. RCU clock security system CSS is connected to NMI vector	0x0000_0008
-1	Fixed	HardFault	Fault Handling Exception	0x0000_000C
-	-	-	Reserved	0x0000_0010 0x0000_0014

Priority	Priority type	Name	Description	Address
				0x0000_0018 0x0000_001C 0x0000_0020 0x0000_0024 0x0000_0028
3	Can set	SVCall	System service called by SVC instruction	0x0000_002C
-	-	-	Reserved	0x0000_0030 0x0000_0034
4	Can set	PendSV	Pending system service	0x0000_0038
5	Can set	SysTick	System tick timer	0x0000_003C
6	Can set	I2C	I2C interrupt	0x0000_0040
7	Can set	HSC	HSC interrupt	0x0000_0044
8	Can set	UART	UART interrupt	0x0000_0048
-	-	-	Reserved	0x0000_004C
9	Can set	WWDT	Window watchdog interrupt	0x0000_0050
10	Can set	TMR0	Timer 0 interrupt	0x0000_0054
11	Can set	TMR1	Timer 1 interrupt	0x0000_0058
12	Can set	C-ADC	C-ADC interrupt	0x0000_005C
13	Can set	V-ADC	V-ADC interrupt	0x0000_0060
14	Can set	FLASH	FLASH interrupt	0x0000_0064
15	Can set	WUPT	Timer wake-up interrupt	0x0000_0068
16	Can set	I2C_STA	I2C start bit interrupt	0x0000_006C
17	Can set	EINT0	External Interrupt 0	0x0000_0070
18	Can set	EINT1	External Interrupt 1	0x0000_0074
19	Can set	EINT2	External Interrupt 2	0x0000_0078
20	Can set	SHA256	SHA256 interrupt	0x0000_007C

7 External Interrupt Controller (EINT)

7.1 Full Name and Abbreviation Description of Terms

Table 13 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Non Maskable Interrupt	NMI

7.2 Introduction

The external interrupt refers to the interrupt caused by the input signal from the I/O pin.

7.3 Main characteristics

(1) Each interrupt has an independent enable control

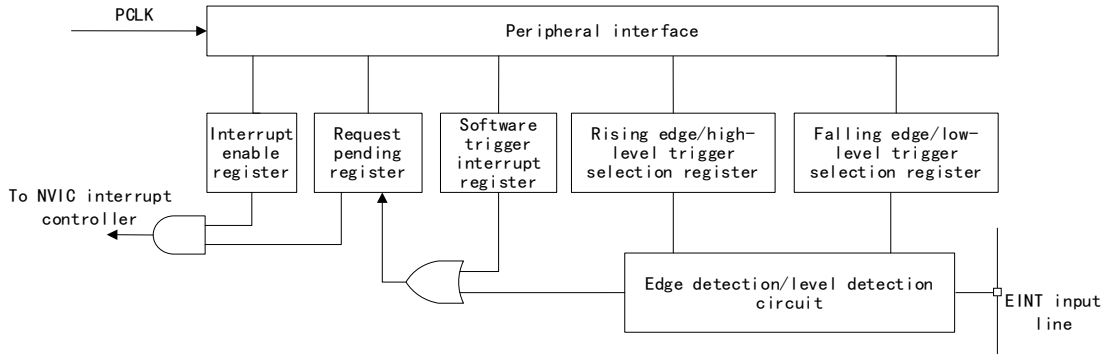
(2) Each interrupt has dedicated status bit

(3) It supports software to trigger interrupt requests

(4) Configurable input dejitter filtering parameters

7.4 Structure block diagram

Figure 6 Structure Block Diagram



7.5 Functional description

The external interrupt controller consists of three interrupt request levels and the edge detectors, and these three lines can be configured to GPIO port. Each input line can independently configure the input type (level or edge), and can be independently enabled. The pending register holds the interrupt requests from the input lines.

7.6 Register address mapping

Table 14 EINT Register Address Mapping

Register name	Description	Offset address
CTRL	Control register	0x00
IEN	Interrupt enable register	0x04
SR	Status register	0x08
SCR	Status clear register	0x0C

7.7 Register functional description

7.7.1 Control register (CTRL)

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	SOFT0	R/W	Software Request 0 1 indicates software request triggering, and 0 indicates no activity
3:1	TRIG_CFG0	R/W	Trigger Configuration 000: High level 001: Low level 010: Rising edge 011: Falling edge 1xx: Double edge
5:4	FILTER_CFG0	R/W	Filter Configuration 00: 0 01: 1 10: 2 11: 3
7:6	DIV_CFG0	R/W	Division Configuration 00: bypass 01: 1/2 frequency division 10: 1/4 frequency division 11: 1/8 frequency division
8	EN0	R/W	EINT0 Enable The module enable signal 1 enables the filter, detection circuit, and frequency dividing circuit
9	SOFT1	R/W	Software Request 1 1 indicates software request triggering, and 0 indicates no activity
12:10	TRIG_CFG1	R/W	Trigger Configuration 000: High level 001: Low level 010: Rising edge

Field	Name	R/W	Description
			011: Falling edge 1xx: Double edge
14:13	FILTER_CFG1	R/W	Filter Configuration 00: 0 01: 1 10: 2 11: 3
16:15	DIV_CFG1	R/W	Division Configuration） 00: bypass 01: 1/2 frequency division 10: 1/4 frequency division 11: 1/8 frequency division
17	EN1	R/W	EINT1 Enable The module enable signal 1 enables the filter, detection circuit, and frequency dividing circuit
18	SOFT2	R/W	Software Request 2 1 indicates software request triggering, and 0 indicates no activity
21:19	TRIG_CFG2	R/W	Trigger Configuration 000: High level 001: Low level 010: Rising edge 011: Falling edge 1xx: Double edge
23:22	FILTER_CFG2	R/W	Filter Configuration 00: 0 01: 1 10: 2 11: 3
25:24	DIV_CFG2	R/W	Division Configuration） 00: bypass 01: 1/2 frequency division 10: 1/4 frequency division 11: 1/8 frequency division
26	EN2	R/W	EINT2 Enable The module enable signal 1 enables the filter, detection circuit, and frequency dividing circuit
31:27	Reserved		

7.7.2 Interrupt enable register (IEN)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	ENABLE_IRQ0	R/W	Interrupt Request 0 Enable 1 represents interrupt enabled, and 0 represents interrupt disabled
1	ENABLE_IRQ1	R/W	Interrupt Request 1 Enable

Field	Name	R/W	Description
			1 represents interrupt enabled, and 0 represents interrupt disabled
2	ENABLE_IRQ2	R/W	Interrupt Request 2 Enable 1 represents interrupt enabled, and 0 represents interrupt disabled
31:3	Reserved		

7.7.3 State register (SR)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	STATE0	R	State0 1 indicates request triggering interrupt, and 0 indicates no activity
1	STATE1	R	State1 1 indicates request triggering interrupt, and 0 indicates no activity
2	STATE2	R	State2 1 indicates request triggering interrupt, and 0 indicates no activity
31:3	Reserved		

7.7.4 State clear register (SCR)

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	SCR0	W1R0	State Clear0 Write 1 to clear the state register, and it can be automatically cleared to 0
1	SCR1	W1R0	State Clear1 Write 1 to clear the state register, and it can be automatically cleared to 0
2	SCR2	W1R0	State Clear2 Write 1 to clear the state register, and it can be automatically cleared to 0
31:3	Reserved		

Note: W1R0 indicates writing 1 to clear, and reading as 0.

8 Reset Management Unit (RMU)

8.1 Full Name and Abbreviation Description of Terms

Table 15 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Reset	RST
Power-On Reset	POR
Power-Down Reset	PDR
Low-Voltage Reset	LVR
Wakeup	WUP

8.2 Introduction

It supports two types of reset modes: system reset and power reset.

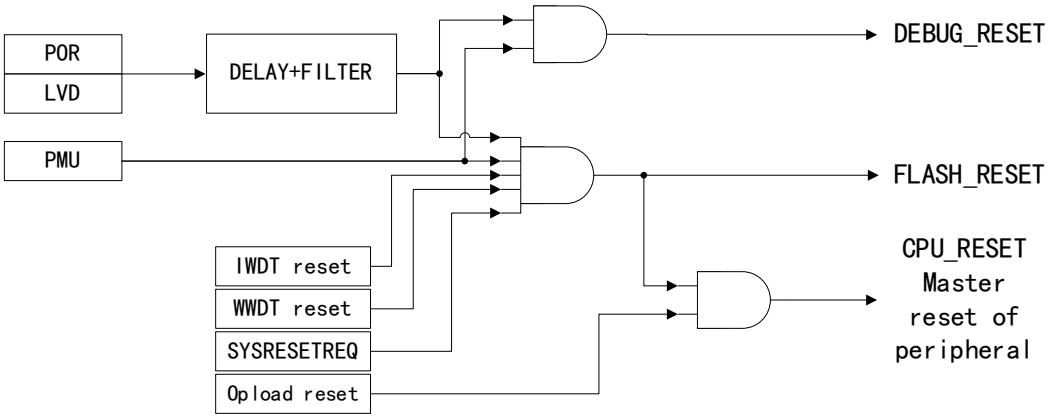
8.3 Main characteristics

(1) It supports tracing of the reset source of the chip

(2) It provides a reset signal synchronized with the work clock for all peripheral modules in the chip

8.4 Structure block diagram

Figure 7 Structure Block Diagram



8.5 Functional description

8.5.1 System reset

System reset will reset the register to the reset state. Users can view the corresponding reset source by querying the SYSCTRL_RSTSR register.

When any of the following events occur, a system reset will be generated:

- Window watchdog event (WWDT)
- Independent watchdog event (IWDT)
- Software reset
- Opload reset

Software reset: Software reset of the core and the peripheral can be achieved by setting the SYSRESTREQ bit in the "Application Interrupt and Reset Control Register" of the core to 1. The other control bit VECTRESET in this register only resets the core and does not reset the peripheral.

Opload reset: The option byte will be forcibly updated, this operation will trigger a system reset, but the system reset will not reset the registers of the FLASH module.

8.5.2 Power reset

When any of the following events occurs, a power reset will occur:

- Power-on reset (POR)
- Power-down reset (PDR)
- Low-voltage reset (LVR)
- When exiting from the low-power HIBERNATE state

Power-on reset: There is a complete power-on reset circuit inside the chip. When the supply voltage reaches V_{por}, the system can work normally. When the supply voltage is lower than the specified limit voltage, the system remains in a reset state.

Power-down reset: When the power supply is unexpectedly interrupted or drops below the PDR threshold, the system enters a reset state.

Low-voltage reset: Low-voltage reset (LVR) is a mandatory protection reset, which can be enabled through the user code option "OP_LVR". When the supply voltage is lower than V_{lvr}, the MCU will generate a reset.

When the system exits from the HIBERNATE low-power state, the entire digital logic will be reset. At this point, the SYSCTRL_STA register will recover to the value before entering HIBERNATE, and the wake-up flag STA_WUF will be set to 1.

8.6 Register address mapping

Related registers:

- SYSCTRL_AHBRSTCR
- SYSCTRL_APBRSTCR
- SYSCTRL_RSTSR
- SYSCTRL_RSTSRCLR

Refer to Register Address Mapping in "System Control (SYSCTRL)".

8.7 Register functional description

Refer to Register Function Description in "System Control (SYSCTRL)".

9 Power Management Unit (PMU)

9.1 Full Name and Abbreviation Description of Terms

Table 16 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Power Management Unit	PMU
Power On Reset	POR
Low Voltage Detector	LVD
Low Voltage Reset	LVR
Low Dropout Regulator	LDO
Low Power Band Gap	LPBG
Low Power Mode	LPM
Power On Reset Brown Out Reset	PORBOR

9.2 Introduction

The power supply is the foundation for stable system operation, and the operating voltage of the chip is 2.0V~5.5V.

9.3 Main characteristics

(1) The internal voltage regulator provides the core operating voltage, supporting low power consumption and normal power consumption states.

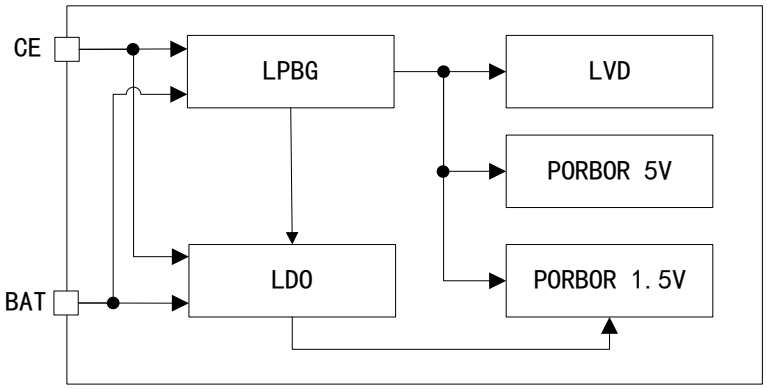
(2) Support LVR (low-voltage reset).

(3) Support LVD (low-voltage detection).

(4) Provide active power-on reset (POR) for power outage detection.

9.4 Structure block diagram

Figure 8 Structure Block Diagram



9.5 Functional description

The chip supports multiple power consumption modes, and the software can select appropriate low-power state in suitable scenarios, to balance the requirements of different power consumption, performance, wake-up time, and wake-up conditions.

After power-on reset, the chip runs in the ACTIVE state by default. At this time, the CPU normally fetches instructions from FLASH, and all peripheral modules can work normally.

9.5.1 Operating mode

Supported working modes: Normal, Sleep, DeepSleep, and Hibernate.

Supported low-power states: WAIT, SLEEP, DPSLEEP, and HIBERNATE. The normal state is ACTIVE. The non-working state is OFF.

Figure 9 Working Mode Diagram

Normal	WAIT	ACTIVE	WAIT	ACTIVE	WAIT	ACTIVE
Sleep	SLEEP	ACTIVE	SLEEP	ACTIVE	SLEEP	ACTIVE
DeepSleep	DPSLEEP	ACTIVE	DPSLEEP	ACTIVE	DPSLEEP	ACTIVE
Hibernate	HIBERNATE					

Different working modes contain different working states:

- Normal mode: Contain WAIT and ACTIVE states.
- Sleep mode: Contain SLEEP and ACTIVE states.
- DeepSleep mode: Contain DPSLEEP and ACTIVE states.
- Hibernate mode: Always in HIBERNATE state.

There are three ways for the system to enter the low-power state:

- WFE instruction
- WFI instruction
- Sleep-On-Exit function

9.5.2 Power consumption state

Table 17 Power Consumption State and Wake-up Mechanism

Power consumption state	Wake-up conditions	Chip status	Wake-up time
ACTIVE	-	-	-
WAIT (SLEEPDEEP=1)	IWDT, WUPT interrupt wake-up STA start bit event wake-up End of C-ADC/V-ADC conversion	Except for IWDT/WUPT, C-ADC and V-ADC, TMR0/1 and UART, all other peripheral clocks of the digital module are turned off. FLASH enters a low-power state. (To further reduce the power consumption in WAIT state, the clock gating of TMR0/1 and UART can be manually turned off before the system enters the WAIT state) The low power consumption state of LDO can be turned on or not.	-
SLEEP (SLEEPDEEP=1)	IWDT, WUPT interrupt wake-up STA start bit event wake-up End of C-ADC/V-ADC conversion	Except for IWDT/WUPT, all other peripheral clocks of the digital module are turned off. LDO low-power mode can be turned on or not, and FLASH enters the low-power mode.	-
DPSLEEP (SLEEPDEEP=1)	IWDT, WUPT interrupt wake-up STA start bit event wake-up End of C-ADC/V-ADC conversion	Except for IWDT/WUPT, all other peripheral clocks of the digital module are turned off. HSICLK enters the low-frequency low-power mode. LDO low-power mode can be turned on or not, and FLASH enters the low-power mode.	150us
HIBERNATE (SLEEPDEEP=1)	STA start bit event wake-up	Both LDO 1.5V and HSICLK are turned off. PMU is on and LSICLK can be turned off or not Other analog modules can be disabled.	20 ms

Power consumption state	Wake-up conditions	Chip status	Wake-up time
OFF	CE is pulled high	Internal 5V output, but peripherals are not enabled.	-

9.5.2.1 WAIT state

Enter WAIT

(1) Set LPM to 00, configure LPE to 1, and start the low-power process.

(2) Execute the WFI/WFE instruction, set SLEEPDEEP=1, the CPU will enter sleep mode, and the PMU will turn off the clocks of other corresponding modules.

Note: If FLASH is executing an erase program, the FLASH clock will not be turned off, and after the erase is completed, it will be automatically turned off, and the LDO/HSICLK low-power state cannot be enabled in the FLASH erase process.

Exit WAIT

(1) When a specific interrupt event occurs, the PMU turns on the clock of the corresponding module.

(2) The CPU is awakened, and according to software configuration, it can enter the interrupt service program or not enter after awakened.

9.5.2.2 SLEEP state

Enter SLEEP

(1) Set LPM to 01, configure LPE to 1, and start the low-power process.

(2) Execute the WFI/WFE instruction, set SLEEPDEEP=1, the CPU will enter sleep mode, and the PMU will turn off the clocks of other corresponding modules.

Note: If FLASH is executing an erase program, the FLASH clock will not be turned off, and after the erase is completed, it will be automatically turned off, and the LDO/HSICLK low-power mode cannot be enabled in the FLASH erase process. .

Exit SLEEP

(1) When a specific interrupt event occurs, the PMU turns on the clock of the corresponding module.

(2) The CPU is awakened, and according to software configuration, it can enter the interrupt service program or not enter after awakened.

9.5.2.3 DPSLEEP state

Enter DPSLEEP

(1) Set LPM to 10, configure LPE to 1, and start the low-power process.

(2) Execute the WFI/WFE instruction, set SLEEPDEEP=1, the CPU will enter sleep mode, and the PMU will turn off the clocks of other corresponding modules.

Note: If FLASH is executing an erase program, the FLASH clock will not be turned off, and after the erase is completed, it will be automatically turned off, and the LDO/HSICLK low-power mode cannot be enabled in the FLASH erase process.

Exit DPSLEEP

(1) When a specific interrupt event occurs, the PMU turns on the clock of the corresponding module.

(2) The CPU is awakened, and according to software configuration, it can enter the interrupt service program or not enter after awakened.

9.5.2.4 HIBERNATE state

Enter HIBERNATE

(1) Ensure that the software does not execute any transactions or that no transactions are being processed.

(2) Set LPM to 11, configure LPE to 1, and start the low-power process.

(3) Enable STA wake-up and configure the wake-up mode as I2C or HSC.

(4) Execute WFI/WFE instructions, set SLEEPDEEP=1, and the CPU will enter sleep.

(5) LDO/HSICLK clock is turned off.

Exit HIBERNATE

(1) I2C/HSC start bit interrupt is detected, and SCL pin is pulled down.

(2) Start LDO and HSICLK, and the reset circuit.

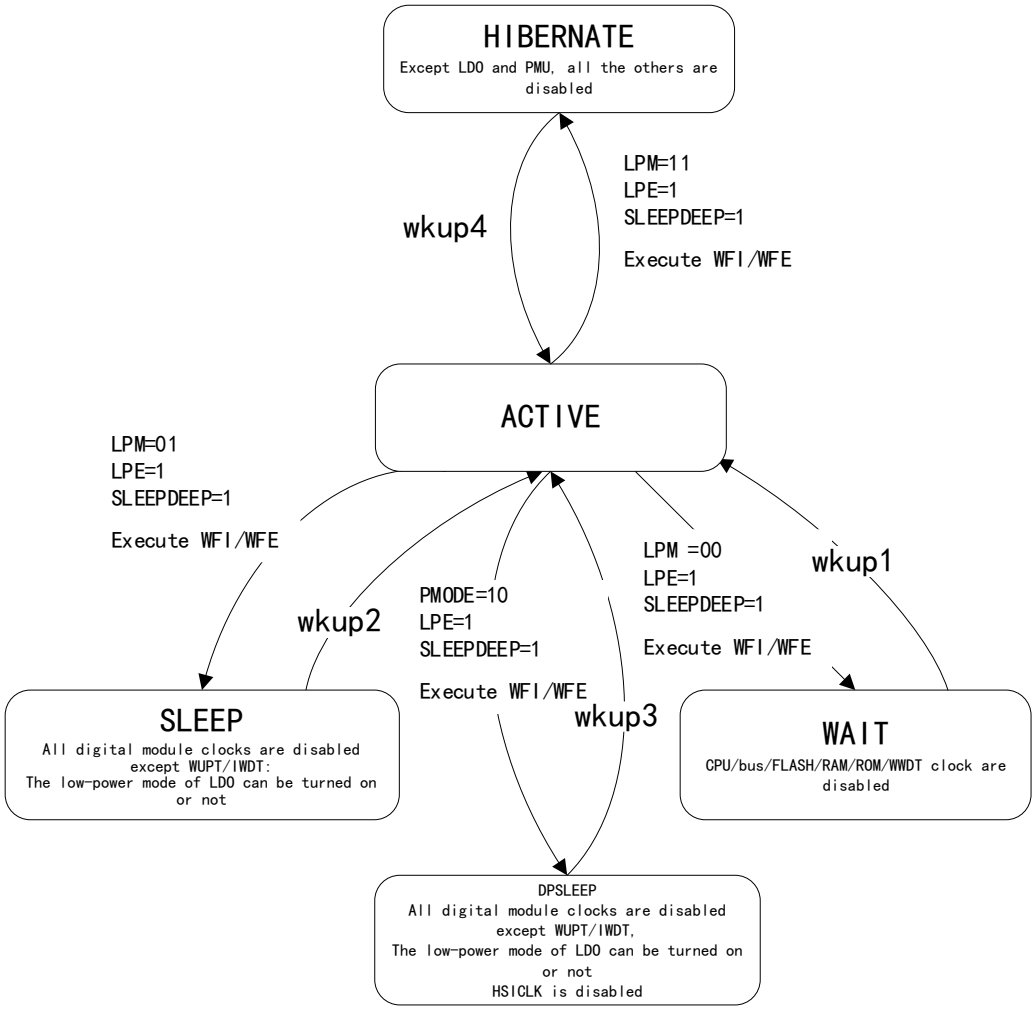
(3) The CPU boots the execution program again and enters the interrupt release SCL/SDA pin, or automatically releases the SCL/SDA pin.

9.5.3 State switching

Different signals can trigger different states.

After the chip is awakened from the HIBERNATE state, the software can quickly identify the current wake-up source by querying relevant registers of the PMU. It is necessary to enter each peripheral module to finish clearing each wake-up source separately.

Figure 10 State Switching Diagram



Note:

(1) wkup1/2/3/4 indicates the wake-up source in different low-power states.

(2) Through PRIMASK function of the Arm® Cortex®-M0+, the chip can wake up with interrupt events, but the CPU does not execute the interrupt handling program. After wake-up, the CPU will continue to run from the instructions before sleep.

9.6 Register address mapping

Related registers:

- SYSCTRL_LPMCR
- SYSCTRL_LPCR

Refer to Register Address Mapping in "System Control (SYSCTRL)".

9.7 Register functional description

Refer to Register Function Description in "System Control (SYSCTRL)".

10 General-Purpose Input/Output Pin (GPIO)

10.1 Full Name and Abbreviation Description of Terms

Table 18 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
P-channel Metal Oxide Semiconductor	P-MOS
N-channel Metal Oxide Semiconductor	N-MOS
General-Purpose Input/Output	GPIO

10.2 Introduction

When the pin is configured as GPIO, the input and output can be controlled through software, and the processor core can communicate with the outside.

10.3 Main characteristics

(1) Embedded with 9 GPIO pins

(2) Options for pin input: Floating, pull-up/pull-down, analog

(3) Options for pin output: Push-pull, open-drain, pull-up/pull-down

(4) Most GPIO pins are shared with multiplexed peripherals

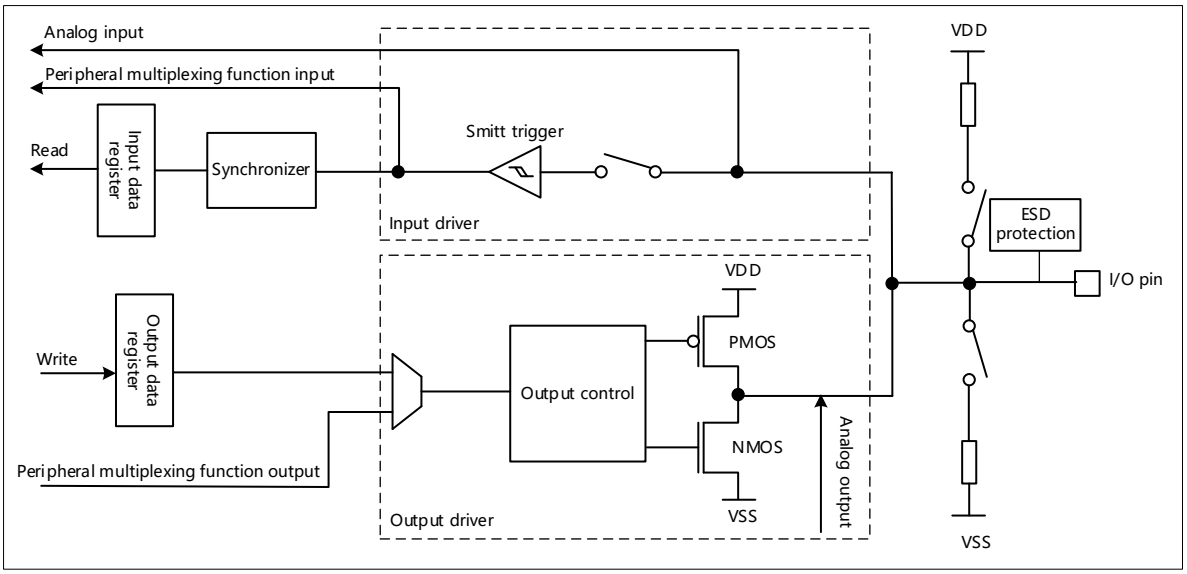
(5) Some pins have redefinition function

(6) Configurable output speed

(7) Configurable output drive strength

10.4 Structure block diagram

Figure 11 Structure Block Diagram



10.5 Functional description

(1) Independent registers are used for data input and output.

(2) External interrupts can be enabled and disabled separately.

(3) Each I/O port can be programmed freely, but the I/O port registers must be accessed in 32-bit words (half-byte access is not allowed).

(4) The output speed control is used to reduce EMC noise.

(5) Multiplexing of I/O functions of on-chip peripherals.

(6) When used as an analog input, the input Schmitt trigger can be turned off to reduce power consumption.

(7) When data output is latched, the sequence of first reading, then modifying, and then writing is supported.

(8) Some pins can be redefined, such as analog input, external interrupt, and input/output of chip peripherals, but only one function can be mapped to a pin at a time. Remapping of multiplexing function can be achieved by controlling the option bytes.

10.6 Register address mapping

Table 19 GPIO Register Address Mapping

Register name	Description	Offset address
GPIO_MDR	Mode register	0x00
GPIO_PUPDR	Pull up and down register	0x04
GPIO_OTR	Output type register	0x08
GPIO_OSR	Output speed register	0x0C
GPIO_DSR	Drive strength register	0x10
GPIO_DINR	Input data register	0x14
GPIO_DOUTR	Output data register	0x18
GPIO_AFSELR	Alternate function select register	0x1C

10.7 Register functional description

10.7.1 Mode register (GPIO_MDR)

Offset address: 0x00

Reset value: 0x0000 000F

Field	Name	R/W	Description
1:0	GPIO0_MD	R/W	GPIO0 Mode 00: Analog mode 01: Digital input mode 10: Digital output mode 11: Multiplexing mode
3:2	GPIO1_MD	R/W	GPIO1 Mode 00: Analog mode 01: Digital input mode 10: Digital output mode 11: Multiplexing mode
5:4	GPIO2_MD	R/W	GPIO2 Mode 00: Analog mode 01: Digital input mode 10: Digital output mode 11: Multiplexing mode
7:6	GPIO3_MD	R/W	GPIO3 Mode 00: Analog mode 01: Digital input mode 10: Digital output mode 11: Multiplexing mode
9:8	GPIO4_MD	R/W	GPIO4 Mode 00: Analog mode 01: Digital input mode

Field	Name	R/W	Description
			10: Digital output mode 11: Multiplexing mode
11:10	GPIO5_MD	R/W	GPIO5 Mode 00: Analog mode 01: Digital input mode 10: Digital output mode 11: Multiplexing mode
13:12	GPIO6_MD	R/W	GPIO6 Mode 00: Analog mode 01: Digital input mode 10: Digital output mode 11: Multiplexing mode
15:14	GPIO7_MD	R/W	GPIO7 Mode 00: Analog mode 01: Digital input mode 10: Digital output mode 11: Multiplexing mode
17:16	Reserved		
19:18	GPIO9_MD	R/W	GPIO9 Mode 00: Analog mode 01: Digital input mode 10: Digital output mode 11: Multiplexing mode
31:20	Reserved		

Note: WLCSP12 and DFN12 are packaged using GPIO0~ GPIO4. QFN16 is packaged using GPIO0~GPIO7 and GPIO9.

10.7.2 Pull up/down register (GPIO_PUPDR)

Offset address: 0x04

Reset value: 0x0000 000D

Field	Name	R/W	Description
0	GPIO0_PUE	R/W	GPIO0 Pull Enable 0: Disable pull up and down 1: Enable pull up and down Note: The default value corresponds to multiplexing SWDIO, internally pulling up
1	GPIO0_PUS	R/W	GPIO0 Pull Select 0: Pull up 1: Pull down Note: It takes effect after pull up and down is enabled. The default value corresponds to multiplexing SWDIO, internally pulling up
2	GPIO1_PUE	R/W	GPIO1 Pull Enable 0: Disable pull up and down 1: Enable pull up and down

Field	Name	R/W	Description
			Note: The default value corresponds to multiplexing SWCLK, internally pulling down
3	GPIO1_PUS	R/W	GPIO1 Pull Select 0: Pull up 1: Pull down Note: It takes effect after pull up and down is enabled. The default value corresponds to multiplexing SWCLK, internally pulling down
4	GPIO2_PUE	R/W	GPIO2 Pull Enable 0: Disable pull up and down 1: Enable pull up and down
5	GPIO2_PUS	R/W	GPIO2 Pull Select 0: Pull up 1: Pull down Note: It takes effect after pull up and down is enabled
6	GPIO3_PUE	R/W	GPIO3 Pull Enable 0: Disable pull up and down 1: Enable pull up and down
7	GPIO3_PUS	R/W	GPIO3 Pull Select 0: Pull up 1: Pull down Note: It takes effect after pull up and down is enabled
8	GPIO4_PUE	R/W	GPIO4 Pull Enable 0: Disable pull up and down 1: Enable pull up and down
9	GPIO4_PUS	R/W	GPIO4 Pull Select 0: Pull up 1: Pull down Note: It takes effect after pull up and down is enabled
10	GPIO5_PUE	R/W	GPIO5 Pull Enable 0: Disable pull up and down 1: Enable pull up and down
11	GPIO5_PUS	R/W	GPIO5 Pull Select 0: Pull up 1: Pull down Note: It takes effect after pull up and down is enabled
12	GPIO6_PUE	R/W	GPIO6 Pull Enable 0: Disable pull up and down 1: Enable pull up and down
13	GPIO6_PUS	R/W	GPIO6 Pull Select 0: Pull up 1: Pull down Note: It takes effect after pull up and down is enabled
14	GPIO7_PUE	R/W	GPIO7 Pull Enable 0: Disable pull up and down 1: Enable pull up and down

Field	Name	R/W	Description
15	GPIO7_PUS	R/W	GPIO7 Pull Select 0: Pull up 1: Pull down Note: It takes effect after pull up and down is enabled
17:16	Reserved		
18	GPIO9_PUE	R/W	GPIO9 Pull Enable 0: Disable pull up and down 1: Enable pull up and down
19	GPIO9_PUS	R/W	GPIO9 Pull Select 0: Pull up 1: Pull down Note: It takes effect after pull up and down is enabled
31:20	Reserved		

Note: WLCSP12 and DFN12 are packaged using GPIO0~ GPIO4. QFN16 is packaged using GPIO0~GPIO7 and GPIO9.

10.7.3 Output type register (GPIO_OTR)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	GPIO0_OT	R/W	GPIO0 Output Type 0: Push-pull 1: Open-drain
1	GPIO1_OT	R/W	GPIO1 Output Type 0: Push-pull 1: Open-drain
2	GPIO2_OT	R/W	GPIO2 Output Type 0: Push-pull 1: Open-drain
3	GPIO3_OT	R/W	GPIO3 Output Type 0: Push-pull 1: Open-drain
4	GPIO4_OT	R/W	GPIO4 Output Type 0: Push-pull 1: Open-drain
5	GPIO5_OT	R/W	GPIO5 Output Type 0: Push-pull 1: Open-drain
6	GPIO6_OT	R/W	GPIO6 Output Type 0: Push-pull 1: Open-drain
7	GPIO7_OT	R/W	GPIO7 Output Type 0: Push-pull 1: Open-drain

Field	Name	R/W	Description
8	Reserved		
9	GPIO9_OT	R/W	GPIO9 Output Type 0: Push-pull 1: Open-drain
31:10	Reserved		

Note: WLCSP12 and DFN12 are packaged using GPIO0~ GPIO4. QFN16 is packaged using GPIO0~GPIO7 and GPIO9.

10.7.4 Output speed register (GPIO_OSR)

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	GPIO0_OS	R/W	GPIO0 Output Speed 0: High speed 1: Low speed
1	GPIO1_OS	R/W	GPIO1 Output Speed 0: High speed 1: Low speed
2	GPIO2_OS	R/W	GPIO2 Output Speed 0: High speed 1: Low speed
3	GPIO3_OS	R/W	GPIO3 Output Speed 0: High speed 1: Low speed
4	GPIO4_OS	R/W	GPIO4 Output Speed 0: High speed 1: Low speed
5	GPIO5_OS	R/W	GPIO5 Output Speed 0: High speed 1: Low speed
6	GPIO6_OS	R/W	GPIO6 Output Speed 0: High speed 1: Low speed
7	GPIO7_OS	R/W	GPIO7 Output Speed 0: High speed 1: Low speed
8	Reserved		
9	GPIO9_OS	R/W	GPIO9 Output Speed 0: High speed 1: Low speed
31:10	Reserved		

Note: WLCSP12 and DFN12 are packaged using GPIO0~ GPIO4. QFN16 is packaged using GPIO0~GPIO7 and GPIO9.

10.7.5 Drive strength register (GPIO_DSR)

Offset address: 0x10

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	GPIO0_DS	R/W	GPIO0 Drive Strength 0: High drive 1: Low drive
1	GPIO1_DS	R/W	GPIO1 Drive Strength 0: High drive 1: Low drive
2	GPIO2_DS	R/W	GPIO2 Drive Strength 0: High drive 1: Low drive
3	GPIO3_DS	R/W	GPIO3 Drive Strength 0: High drive 1: Low drive
4	GPIO4_DS	R/W	GPIO4 Drive Strength 0: High drive 1: Low drive
5	GPIO5_DS	R/W	GPIO5 Drive Strength 0: High drive 1: Low drive
6	GPIO6_DS	R/W	GPIO6 Drive Strength 0: High drive 1: Low drive
7	GPIO7_DS	R/W	GPIO7 Drive Strength 0: High drive 1: Low drive
8	Reserved		
9	GPIO9_DS	R/W	GPIO9 Drive Strength 0: High drive 1: Low drive
31:10	Reserved		

Note: WLCSP12 and DFN12 are packaged using GPIO0~ GPIO4. QFN16 is packaged using GPIO0~GPIO7 and GPIO9.

10.7.6 Input data register (GPIO_DINR)

Offset address: 0x14

Reset value: 0x0000 0001

Field	Name	R/W	Description
0	GPIO0_DIN	R	PAD0 Data Input
1	GPIO1_DIN	R	PAD1 Data Input
2	GPIO2_DIN	R	PAD2 Data Input

Field	Name	R/W	Description
3	GPIO3_DIN	R	PAD3 Data Input
4	GPIO4_DIN	R	PAD4 Data Input
5	GPIO5_DIN	R	PAD5 Data Input
6	GPIO6_DIN	R	PAD6 Data Input
7	GPIO7_DIN	R	PAD7 Data Input
8	Reserved		
9	GPIO9_DIN	R	PAD9 Data Input
31:10	Reserved		

Note: WLCSP12 and DFN12 are packaged using GPIO0~ GPIO4. QFN16 is packaged using GPIO0~GPIO7 and GPIO9.

10.7.7 Output data register (GPIO_DOUTR)

Offset address: 0x18

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	GPIO0_DOUT	R/W	PAD0 Data Output
1	GPIO1_DOUT	R/W	PAD1 Data Output
2	GPIO2_DOUT	R/W	PAD2 Data Output
3	GPIO3_DOUT	R/W	PAD3 Data Output
4	GPIO4_DOUT	R/W	PAD4 Data Output
5	GPIO5_DOUT	R/W	PAD5 Data Output
6	GPIO6_DOUT	R/W	PAD6 Data Output
7	GPIO7_DOUT	R/W	PAD7 Data Output
8	Reserved		
9	GPIO9_DOUT	R/W	PAD9 Data Output
31:10	Reserved		

Note: WLCSP12 and DFN12 are packaged using GPIO0~ GPIO4. QFN16 is packaged using GPIO0~GPIO7 and GPIO9.

10.7.8 Alternate function select register (GPIO_AFSELR)

Offset address: 0x1C

Reset value: 0x0000 0000

Field	Name	R/W	Description
1:0	GPIO0_AFSELR	R/W	GPIO0 Alternate Function Select Enable 00: SWDIO 01: INT0 10: TMR0OUT 11: UART TX

Field	Name	R/W	Description
3:2	GPIO1_AFSELR	R/W	GPIO1 Alternate Function Select Enable 00: SWDCLK 01: INT1 10: TMR1OUT 11: UART RX
5:4	GPIO2_AFSELR	R/W	GPIO2 Alternate Function Select Enable 00: I2C serial clock 01: AF1 10：AF2 11: AF3
7:6	GPIO3_AFSELR	R/W	GPIO3 Alternate Function Select Enable 00: I2C serial data 01：HSC 10：AF2 11: AF3
9:8	GPIO4_AFSELR	R/W	GPIO4 Alternate Function Select Enable 00: AF0 01: INT2 10: SYSTEM_DBG_CLK 11: AF3
11:10	GPIO5_AFSELR	R/W	GPIO5 Alternate Function Select Enable 00: AF0 01: AF1 10：AF2 11: AF3
31:12	Reserved		

11 Timer (TMR0/1)

11.1 Full Name and Abbreviation Description of Terms

Table 20 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Timer	TMR
Pulse-Width Modulation	PWM
Special Function Register	SFR

11.2 Introduction

With the time base unit as the core, the general-purpose timer can generate output waveform.

Two identical timers TMR0/1 run independently. The counter module has a 16-bit programmable prescaler, a 16-bit up counter, and supports 1 PWM output.

11.3 Main characteristics

(1) 16-bit prescaler

(2) 16-bit counter

(3) Configurable PWM duty cycle

(4) Configurable PWM output

(5) Autoreload function

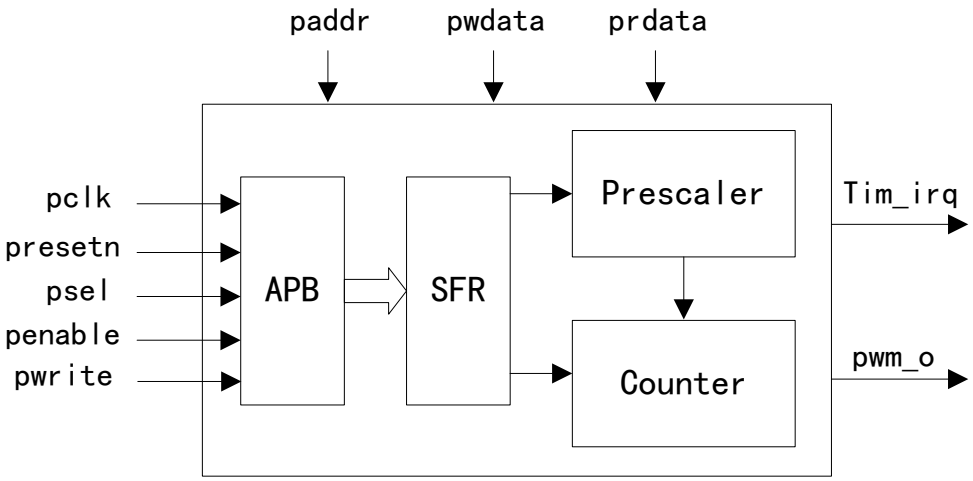
(6) Configurable output polarity

(7) Configurable duty cycle

(8) Overflow interrupt

11.4 Structure block diagram

Figure 12 Structure Block Diagram



11.5 Functional description

11.5.1 TMR mode

The counting unit of this timer is a 16-bit up counter, setting CTRL[MODE]=0, and selecting TMR mode. Select the appropriate prescaler factor by configuring CTRL[PS], and set the maximum count value of the counter by setting the ARV register.

- When CTRL[BUFEN]=0, after the data is written to the ARV register, it will be automatically updated to the shadow register.
- When CTRL[BUFEN]=1, even if the shadow register of the ARV register is enabled, in case of overload, the value written to the ARV register will be updated to the shadow register. But when CTRL[EN] is not enabled, the data written to the ARV register will be updated to the shadow register whether CTRL[BUFEN] is enabled or not.

When the count value of the counter changes from ARV to 0, Overload will occur and the SR[OVC] flag bit will be set. If IEN[SRCIIE] is enabled, an interrupt will occur.

11.5.2 PWM mode

Set CTRL[MODE] to 1 and select PWM mode. Select the appropriate prescaler factor by configuring CTRL[PS], set the PWM period by setting the ARV register, select the polarity of the duty cycle by setting CTRL[PWMXS], and set the duty cycle by configuring the PWMXD register.

- When CTRL[BUFEN]=0, after the data is written to the ARV register and PWMXD register, it will be automatically updated to the shadow register.

- When CTRL[BUFEN]=1, even if the shadow register of the ARV and PWMXD registers is enabled, in case of overload, the value written to the ARV and PWMXD registers will be updated to the shadow register. But when CTRL[EN] is not enabled, the data written to the ARV and PWMXD registers will be updated to the shadow register whether CTRL[BUFEN] is enabled or not.

When the count value reaches the duty cycle register value, the SR[PWMM] flag bit will be set. When the count value of the counter changes from ARV to 0, Overload will occur and the SR[OVC] flag bit will be set. If the corresponding interrupt is enabled, an interrupt will occur.

11.6 Register address mapping

Table 21 TMR Register Address Mapping

Register name	Description	Offset address
CTRL	Control register	0x00
PWMXD	PWM duty cycle register	0x04
ARV	Auto reload register	0x08
CNT	Counter register	0x0C
IEN	Interrupt enable register	0x10
SR	Status register	0x14
SCR	Status clear register	0x18

11.7 Register functional description

11.7.1 Control register (CTRL)

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	EN	R/W	TMR Enable 0: Disable 1: Enable
1	MODE	R/W	Mode 0: TMR 1: PWM
2	PWMXS	R/W	PWM Initial Level 0: Duty cycle output is at a high level 1: Duty cycle output is at a low level
3	BUFEN	R/W	Buffer Enable 0: Disable 1: Enable

Field	Name	R/W	Description
			When this bit is enabled, the values of the PWMXD and ARV registers will be reloaded to the Buffer to take effect when overflows occurs, and will be directly reloaded to the Buffer if this bit is enabled before CTRL[EN] is enabled
7:4	PS	R/W	Prescaler Factor Select 0000: The frequency division factor is 1 0001: The frequency division factor is 2 0010: The frequency division factor is 4 0011: The frequency division factor is 8 0100: The frequency division factor is 16 0101: The frequency division factor is 32 0110: The frequency division factor is 64 0111: The frequency division factor is 128 1000: The frequency division factor is 256 1001: The frequency division factor is 512 1010: The frequency division factor is 1024 Others: The frequency division factor is 1024
31:8	Reserved		

11.7.2 PWM duty cycle register (PWMXD)

Offset address: 0x04

Reset value: 0xFFFF FFFF

Field	Name	R/W	Description
15:0	PWMXD	R/W	PWM Polarity When CNT≤PWM_XD: CTRL[PWMXS]=0 outputs high level CTRL[PWMXS]=1 outputs low level When CNT>PWM_XD: CTRL[PWMXS]=0 outputs low level CTRL[PWMXS]=1 outputs high level When PWMXD=0x0000: CTRL[PWMXS]=0 outputs low level CTRL[PWMXS]=1 outputs high level Note: This register is only valid in PWM mode
31:16	Reserved		

11.7.3 Auto reload ratio register (ARV)

Offset address: 0x08

Reset value: 0xFFFF FFFF

Field	Name	R/W	Description
15:0	ARV	R/W	Auto Reload Value In TMR mode, this value is the maximum count value In PWM mode, this value is the PWM period value
31:16	Reserved		

11.7.4 Counter register (CNT)

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	CNT	R	Counter
31:16	Reserved		

11.7.5 Interrupt enable register (IEN)

Offset address: 0x10

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	OVCIE	R/W	Overload Interrupt Enable 0: Disable 1: Enable
1	PWMMIE	R/W	PWM Match Interrupt Enable 0: Disable 1: Enable
31:2	Reserved		

11.7.6 State register (SR)

Offset address: 0x14

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	OVC	R	Overload Condition Overload flag generated when the count value of the counter changes from the ARV register configuration value to 0
1	PWMM	R	PWM Match Generate a matching flag when the Counter counts to PWMXD in PWM mode Note: It is only valid in PWM mode
31:2	Reserved		

11.7.7 State clear register (SCR)

Offset address: 0x18

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	OVCC	W1R0	Overload Condition Clear It can be cleared by writing 1, and be automatically reset to 0 by hardware
1	PWMMC	W1R0	PWMM Clear It can be cleared by writing 1, and be automatically reset to 0 by hardware
31:2	Reserved		

Note: W1R0 indicates writing 1 to clear, and reading as 0.

12 Watchdog Timer (WDT)

12.1 Full Name and Abbreviation Description of Terms

Table 22 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Independent Watchdog Timer	IWDT
Windows Watchdog Timer	WWDT

12.2 Introduction

The watchdog is used to monitor system faults caused by software errors. The chip is equipped with two watchdog devices: an independent watchdog and a window watchdog. They not only improve the security, but also increase the accuracy of time and flexibility of use.

The independent watchdog will reset only when the counter value is reduced to 0, and the value of refresh counter will not be reset until it is not reduced to 0.

The window watchdog will reset when the counter value decreases to 0. When the count value is before the window value of the configuration register, the counter will be reset after refresh.

12.3 Independent watchdog timer (IWDT)

12.3.1 Introduction

The independent watchdog has an independent clock source, which monitors the running status of the system, and is suitable for situations where an independent environment is required but the requirement for accuracy is not high. Even in the event of the master clock failure, the independent watchdog remains effective and can be used as wake-up in Sleep mode.

12.3.2 Main characteristics

(1) Use the low-frequency auxiliary clock LSICLK as the clock source

(2) Down counter

(3) Can be used as a wake-up source

(4) Overflow triggers reset

(5) Configurable down counter

(6) Configurable clock frequency selection

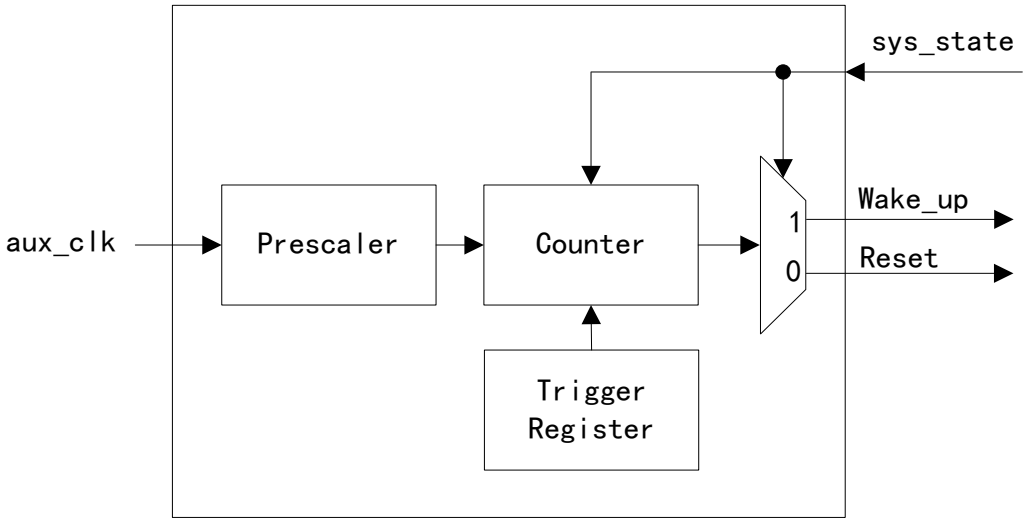
(7) Low-frequency independent clock drive

(8) Support 8-bit counter

(9) Support hardware boot

12.3.3 Structure block diagram

Figure 13 Structure Block Diagram



12.3.4 Functional description

If the watchdog is activated (TRG register of IWDT is configured with 0xCC), a reset will be triggered when the 8-bit down counter (RV[7:0] bit) counts to zero.

The application must periodically write 0xAA to the TRG register during normal operation to prevent system reset.

Enable the watchdog

- When the IWDTEN of Option Byte is set to 0, the watchdog will always be off after the system is reset. The watchdog can be enabled by writing 0xCC to the TRG register, and it cannot be turned off again unless a reset operation is performed.
- When the IWDTEN of Option Byte is set to 1, the enable bit will be loaded from the NVR region after the system is powered on. At this time, even if the TRG register does not write 0xCC, IWDT will still be enabled.

Feed the dog

The dog feeding action of IWDT is to write 0xAA to the TRG register. When the software writes 0xAA to the TRG register, the RV value will be reloaded into the counter, and the counter will start counting again from the reloaded value.

12.3.5 Register address mapping

Table 23 IWDT Register Address Mapping

Register name	Description	Offset address
PS	Prescale register	0x00
TRG	Feed register	0x04
RV	Reload value register	0x08
SR	Status register	0x0C

12.3.6 Register functional description

12.3.6.1 Prescaler register (PS)

Offset address: 0x00

Reset value: 0x0000 000F

Field	Name	R/W	Description
3:0	PS	R/W	Prescaler Factor Select 0000: The frequency division factor is 1 0001: The frequency division factor is 2 0010: The frequency division factor is 4 0011: The frequency division factor is 8 0100: The frequency division factor is 16 0101: The frequency division factor is 32 0110: The frequency division factor is 64 0111: The frequency division factor is 128 1000: The frequency division factor is 256 1001: The frequency division factor is 512 1010: The frequency division factor is 1024 1011: The frequency division factor is 2048 1100: The frequency division factor is 4096 1101: The frequency division factor is 8192 1110: The frequency division factor is 16384 1111: The frequency division factor is 32768
31:4	Reserved		

12.3.6.2 Feed register (TRG)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	TRG	R/W	Trigger Feed the dog when 0xAA is written Unlock the PS and RV registers when 0x55 is written Enable IWDT when 0xCC is written
31:8	Reserved		

12.3.6.3 Reload value register (RV)

Offset address: 0x08

Reset value: 0x0000 00FF

Field	Name	R/W	Description
7:0	RV	R/W	Reload Value
31:8	Reserved		

Note: This register cannot be configured to 0, or it will be invalid.

12.3.6.4 State register (SR)

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	TU	R	Trigger Update Feeding the dog, the hardware will automatically clear it to zero after updating
1	PU	R	PS Update After updating, the hardware will automatically clear it to zero
2	RU	R	Reload Update After updating, the hardware will automatically clear it to zero
31:3	Reserved		

12.4 Window watchdog (WWDT)

12.4.1 Introduction

The window watchdog is suitable for situations where precise timing is required, to detect software failures and abnormal operation of applications. The window watchdog clock comes from PCLK, and the counter clock is obtained from the CK counter clock through frequency division by prescaler. If the window watchdog does not receive feeding operation within the programmed time period, a reset signal will be generated.

12.4.2 Main characteristics

(1) Configurable 16-bit down counter

(2) Programmable prescaler

(3) Configurable interrupt trigger window

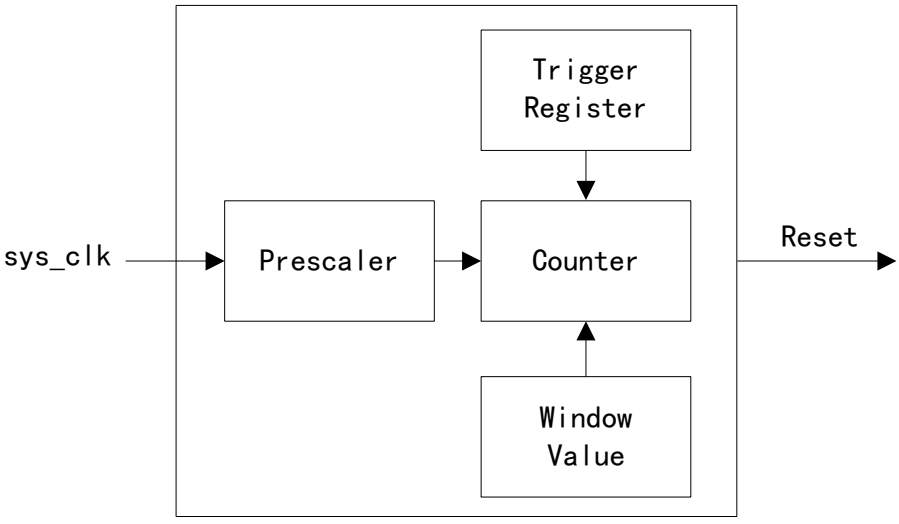
(4) Overflow triggers reset

(5) Configurable clock frequency selection

(6) Hardware boot

12.4.3 Structure block diagram

Figure 14 Structure Block Diagram



12.4.4 Functional description

If the watchdog is activated (the TRG register of WWDT is configured with 0xAA), a reset will be triggered when the 16-bit down counter (RV[15:0] bit) counts to zero. When the counter value is greater than the value stored in the window register, if the software reloads the counter, a reset will occur.

The application must periodically write to the TRG register during normal

operation to prevent system reset. This operation can only be performed when the counter value is lower than the window register value and before the count value is reset.

Enable the watchdog

- When the WWDTEN of Option Byte is set to 0, the watchdog will be always off after the system is reset. The watchdog can be enabled by writing 0xAA to the TRG register, and it cannot be turned off again unless a reset operation is performed.
- When the WWDTEN of Option Byte is set to 1, the enable bit will be loaded from the NVR region after the system is powered on. At this time, even if the TRG register does not write 0xAA, WWDT will still be enabled.

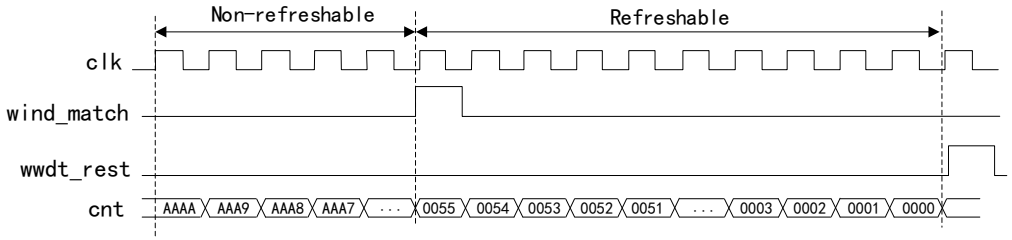
Window mode

The WWDT watchdog register WIND is used to store window values, and the feeding interval of the WWDT watchdog is affected by the WIND register. When the count value is greater than WIND, feeding will occur, and a reset will be generated, so the feeding interval is less than or equal to the WIND value.

Feed the dog

The dog feeding action of WWDT is to write 0xAA to the TRG register. When the software writes 0xAA to the TRG register, the RV value will be reloaded into the counter, and the counter will start counting again from the reloaded value. Configure RV reload value as 0xAAAA and window value as 0x0055 as shown in the following figure.

Figure 15 WWDT Timing Diagram



Interrupt

WWDT can be configured with interrupts. When the count value equals the window value, a WINDMF window value matching flag will be generated. When IEN[WINDMIE] is enabled, an interrupt will be generated. The matching flag and interrupt can be cleared by writing 1 through SCR[WINDMFC].

12.4.5 Register address mapping

Table 24 WWDT Register Address Mapping

Register name	Description	Offset address
PS	Prescale register	0x00
TRG	Feed register	0x04
WIND	Window value register	0x08
RV	Reload data register	0x0C
CNT	Count value register	0x10
IEN	Interrupt enable register	0x14
SR	Status register	0x18
SCR	Status clear register	0x1C

12.4.6 Register functional description

12.4.6.1 Prescaler register (PS)

Offset address: 0x00

Reset value: 0x0000 000F

Field	Name	R/W	Description
3:0	PS	R/W	Prescaler Factor Select 0000: The frequency division factor is 1 0001: The frequency division factor is 2 0010: The frequency division factor is 4 0011: The frequency division factor is 8 0100: The frequency division factor is 16 0101: The frequency division factor is 32 0110: The frequency division factor is 64 0111: The frequency division factor is 128 1000: The frequency division factor is 256 1001: The frequency division factor is 512 1010: The frequency division factor is 1024 1011: The frequency division factor is 2048 1100: The frequency division factor is 4096 1101: The frequency division factor is 8192 1110: The frequency division factor is 16384 1111: The frequency division factor is 32768
31:4	Reserved		

12.4.6.2 Feed register (TRG)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	TRG	R/W	Trigger Feed the dog when 0xAA is written
31:8	Reserved		

12.4.6.3 Window Value Register (WIND)

Offset address: 0x08

Reset value: 0x0000 FFFF

Field	Name	R/W	Description
15:0	WIND	R/W	Window Data
31:16	Reserved		

12.4.6.4 Reload value register (RV)

Offset address: 0x0C

Reset value: 0x0000 FFFF

Field	Name	R/W	Description
15:0	RV	R/W	Reload Value
31:16	Reserved		

12.4.6.5 Count value register (CNT)

Offset address: 0x10

Reset value: 0x0000 FFFF

Field	Name	R/W	Description
15:0	CNT	R	Counter
31:16	Reserved		

12.4.6.6 Interrupt enable register (IEN)

Offset address: 0x14

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	WINDMIE	R/W	Window Match Interrupt Enable 0: Disable 1: Enable
31:1	Reserved		

12.4.6.7 State register (SR)

Offset address: 0x18

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	WINDMF	R	Window Match Flag 1: The count value is equal to the window value 0: The count value is not equal to the window value
31:1	Reserved		

12.4.6.8 State clear register (SCR)

Offset address: 0x1C

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	WINDMFC	W1R0	Window Match Flag Clear

Field	Name	R/W	Description
			Write 1 to clear the state register, and it can be automatically cleared to 0 by hardware
31:1	Reserved		

Note: W1R0 indicates writing 1 to clear, and reading as 0.

13 Wake-Up Timer (WUPT)

13.1 Full Name and Abbreviation Description of Terms

Table 25 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Auto Wake-Up Timer	WUPT

13.2 Introduction

When the MCU enters a low-power state, WUPT can provide an internal wake-up time reference. The clock of this time reference is provided by the crystal oscillator clock LSICLK of the internal low-speed RC oscillator clock.

13.3 Main characteristics

(1) The low-power state (WAIT/SLEEP/DPSLEEP) can provide internal wake-up function

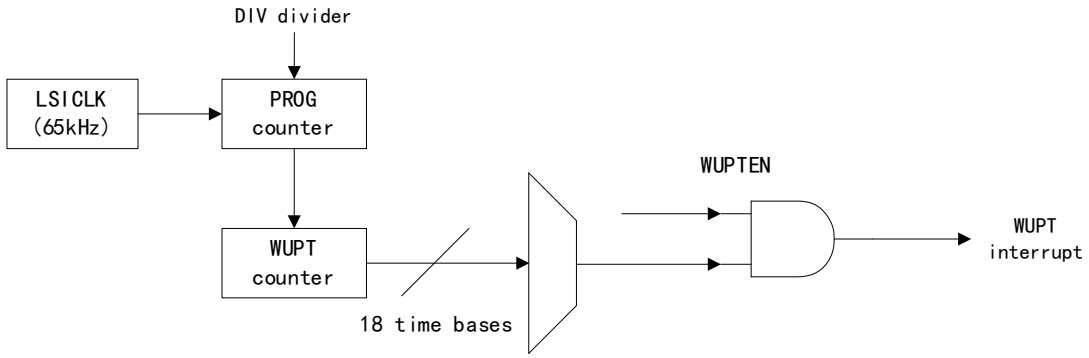
(2) Configure the prescaler value

(3) Configure different time bases

(4) LSICLK serves as the count clock source

13.4 Structure block diagram

Figure 16 Structure Block Diagram



13.5 Functional description

13.5.1 WUPT configuration process

(1) Configure the DIV[5:0] bit of the WUPT_CFG register to define appropriate prescaler value.

(2) Configure the TBC[3:0] bit of the WUPT_CFG register to select the desired automatic wake-up delay.

(3) Configure the WUPTEN bit of the WUPT_CSTS register to enable WUPT function.

(4) Execute the low-power process.

13.5.2 Time base selection

The time interval of WUPT depends on the output column of the counter given by the TBC[17:0] bit, and the DIV[5:0] prescaler factor.

13.6 Register address mapping

Table 26 WUPT Register Address Mapping

Register name	Description	Offset address
WUPT_CSTS	Control state register	0x00
WUPT_CFG	Prescale state register	0x04
WUPT_SCR	Time base selection register	0x08

13.7 Register functional description

13.7.1 Control state register (WUPT_CSTS)

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	WUPTEN	R/W	Auto-wakeup Enable This bit is set to 1 and cleared to 0 by software. If the MCU enters active stop or wait mode, the automatic wake-up module will be preprogrammed to set delay for a period of time before waking up the MCU. 0: Disable 1: Enable
1	WUPIE	R/W	WUPT Interrupt Enable 0: Disable 1: Enable
2	WAKE_STATE	R/W	Wake State 1: WUPT is triggered 0: WUPT is not triggered Note: Clear after writing CLR_STATE
31:3	Reserved		

13.7.2 Prescaler state register (WUPT_CFG)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
5:0	DIV	R/W	Asynchronous Prescaler Division This bit is used to select the division value provided to the counter clock. 0x00: 2 frequency division 0x01: 3 frequency division … 0x06: 8 frequency division … 0x0E: 16 frequency division 0x0F: 17 frequency division … 0x3E: 64 frequency division 0x3F: 65 frequency division
23:6	TBC	R/W	Auto-wakeup Timebase Select This bit is used to define the interval time of automatic wake-up interrupt Basic duration=(1/65K)* (div+2)*(tbc+1)s
31:24	Reserved		

13.7.3 Time base selection register (WUPT_SCR)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	CLR_STATE	R/W	Clear State It can be cleared by writing 1, and be automatically cleared to 0 after the state in the LSICLK field is cleared.
1	CLR_CNT	R/W	Clear Counter It will be automatically cleared to 0 after the counter in the LSICLK field is cleared.
31:2	Reserved		

14 Internal Integrated Circuit Interface (I2C)

14.1 Full Name and Abbreviation Description of Terms

Table 27 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Serial Data	SDA
Serial Clock	SCL
Clock	CLK
Negative Acknowledgement	NACK
Finite State Machine	FSM
Special Function Register	SFR

14.2 Introduction

I2C is a short-distance bus communication protocol. In physical implementation, I2C bus is composed of two signal lines (SDA and SCL) and one ground wire. These two signal lines can be used for bidirectional transmission. SCL provides timing for SDA, and SDA transmits or receives data in series.

14.3 Main characteristics

(1) It is embedded with 1 I2C interface, led out externally through data pin (SDA) and clock pin (SCL), and capable of enabling or disabling interrupts

(2) Support master/slave mode

(3) Support programmable addresses

(4) Support 7-bit addressing

(5) Support connection to standard (up to 100kHz) or fast (up to 400kHz) I2C bus communication rate

(6) Convert serial data to parallel data when receiving data, and convert parallel data to serial data when transmitting data

(7) Low-level timeout judgment

(8) Support broadcast call

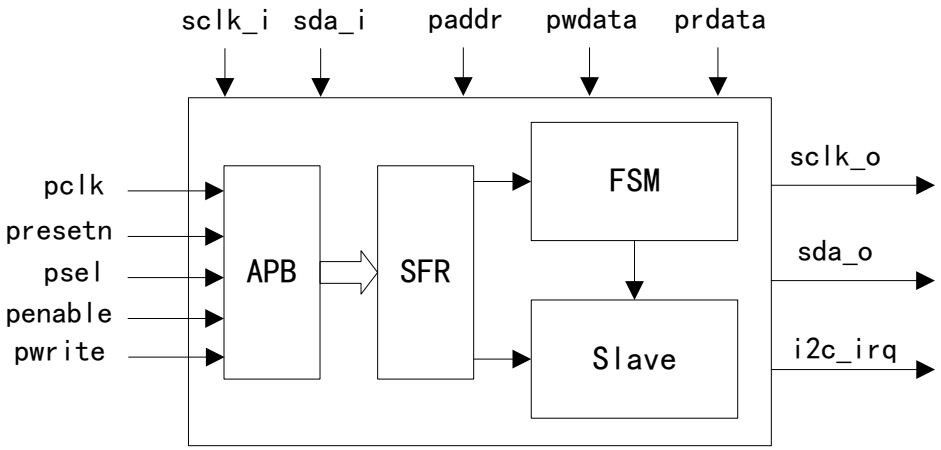
(9) Support multi-master arbitration

(10) Programmable configuration of master clock

(11) Configurable digital filtering

14.4 Structure block diagram

Figure 17 Structure Block Diagram



14.5 Functional description

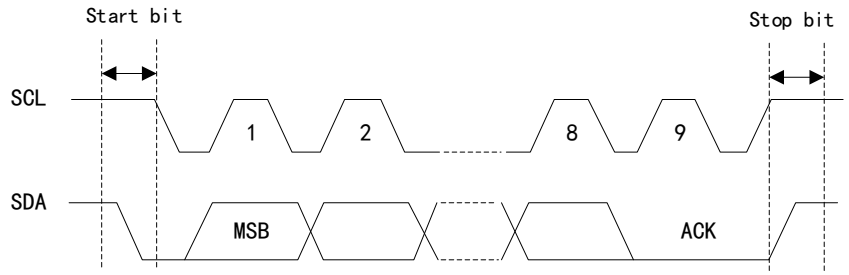
The I2C module is an internal circuit that allows communication with external I2C interfaces. It is a two-wire serial interface that complies with industry standards and is used to connect external hardware. These two serial lines are called the serial data line SDA and the serial clock line SCL.

The SDA line is a bidirectional data line, which connects the entire I2C bus, and is used for data transmission and receiving between the master and the slave. The SCL clock line provides synchronous clock signals for data transmission.

The I2C module provides two data transmission rates: standard mode 100kHz and fast mode 400kHz. The SCLC clock configuration register is used to set different duty cycles so as to obtain different SCL pulses.

The I2C module has arbitration detection function in order to prevent multiple masters from attempting to transmit data to the I2C bus simultaneously.

Figure 18 I2C Bus Protocol



14.5.1 START and STOP conditions

The master can initiate the transmission by sending a START signal and terminate the transmission by sending a STOP signal. The START signal is usually referred to as the "S" bit, defined as the level change from high to low on the SDA line when the SCL line is at a high level. The STOP signal is usually referred to as the "P" bit, defined as the level change from low to high on the SDA line when the SCL line is at a high level.

The repeated START, called the "Sr" bit, has the same function as the START condition. A repeated START signal allows the I2C interface to communicate with other slaves or with the same I2C device in different transmission directions without releasing the bus control.

Figure 19 I2C START Conditions

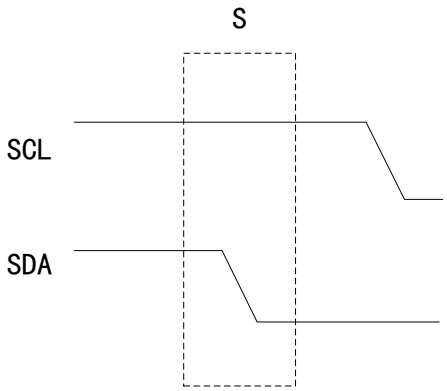
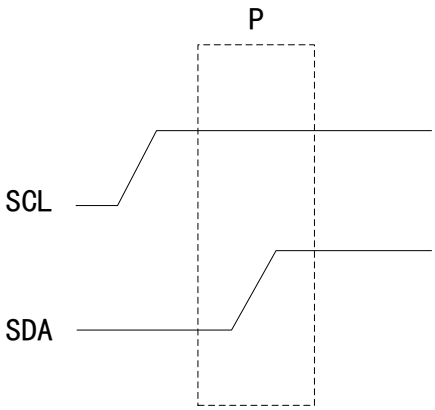


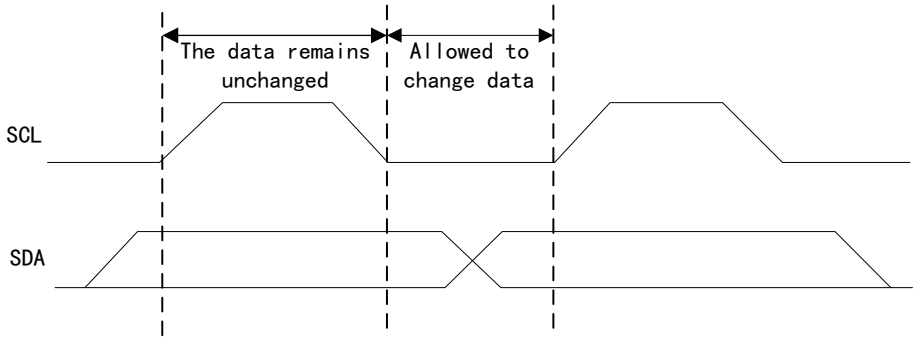
Figure 20 I2C STOP Conditions



14.5.2 Data validity

When transmitting data, the data on the SDA line must remain stable during the high-level period of the SCL clock. The SDA data state can only change when the clock signal on the SCL line is in a low-level state.

Figure 21 Data Validity



14.5.3 Addressing Format

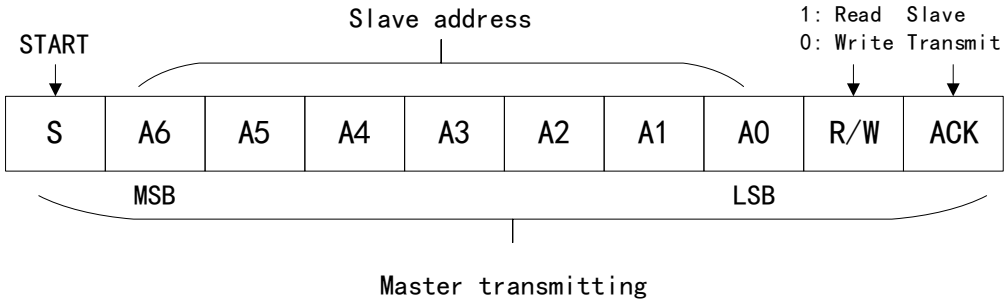
After the master sends the address confirmation to the target slave, the I2C interface starts transmitting data. The address frame is sent out after the master sends the START signal.

The 7-bit address format consists of the following parts: a 7-bit length slave address for communication with the master, an R/W bit, and an ACK bit. The R/W bit defines the direction of data transmission.

- R/W=0 (write): The master sends data to the addressed slave.
- R/W=1 (read): The master receives data from the addressed slave.

The slave address can be allocated through the SADDR register. If the slave address matches the address sent by the master, the slave will return an acknowledgement bit (ACK).

Figure 22 Transmission Address Format



14.5.4 Data transmission and acknowledgment

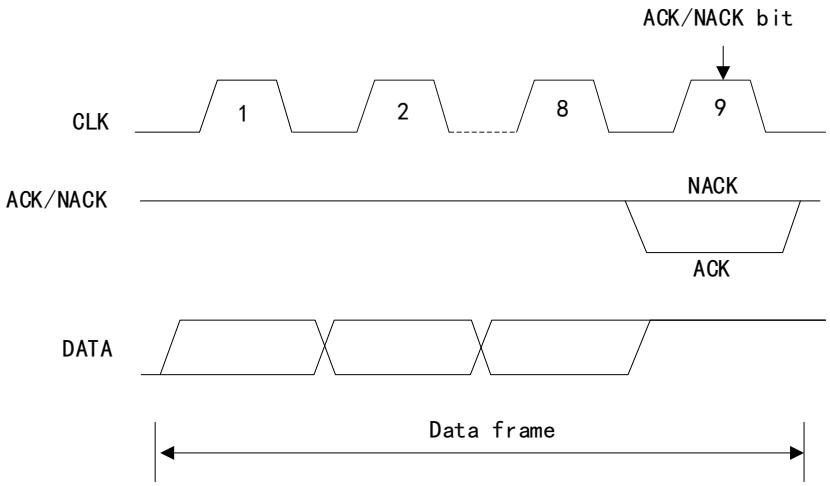
Once the slave address matches, the data can be transmitted or received by the slave based on the transmission direction defined by the R/W bit. Each byte is followed by an acknowledgement bit on the 9th SCL clock.

If the slave returns a non-acknowledgment signal (NACK) to the master, the master will generate a STOP signal to terminate data transmission or generate a repeated START signal to restart transmission.

If the master sends a non-acknowledgment signal (NACK) to the slave, the slave will release the SDA line to the master, and the master will generate a

STOP signal to terminate the transmission.

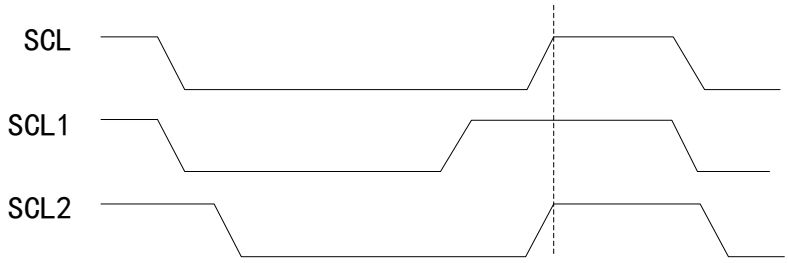
Figure 23 Data Frame Format



14.5.5 Clock synchronization

During normal operation, only one master can generate the SCL clock. However, when multiple masters attempt to generate SCL clocks, the clocks should be synchronized in order to compare the output data. Clock synchronization can be performed through the connection between I2C interface and SCL.

Figure 24 Clock Synchronization



14.5.6 Arbitration

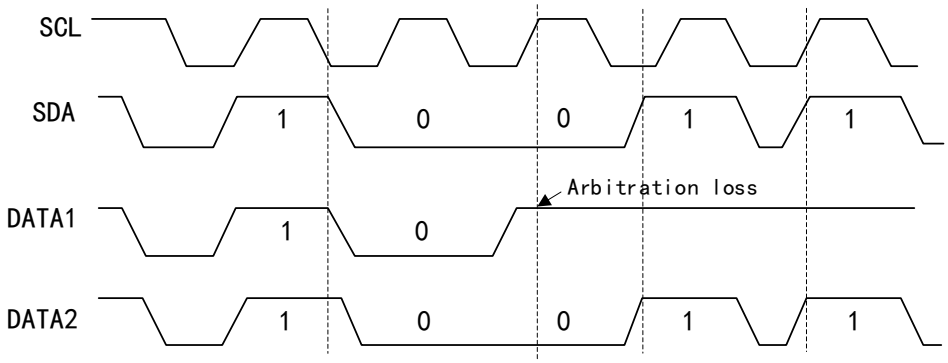
The master can only start transmitting when the I2C bus is in a free or idle state. If two or more masters generate START signals almost simultaneously, an arbitration procedure will occur.

The arbitration occurs on the SDA line and can last for many bits. The arbitration procedure assigns higher priority to the device that sends low serial data. Other masters that want to send high-level data will lose arbitration. As long as the master loses the arbitration, the I2C module will set the ARBLOS bit in the SR register, and generate an interrupt when the interrupt enable bit ARBLOSIE in the IEN register is set to 1.

If the arbitration is lost in the phase of transmitting addresses, it will enter the phase of the Slave receiving addresses, and the device will switch to Slave

mode. If the arbitration is lost in the data transmission phase, it will enter I2C_BUSY. If START is received in this phase, it will enter SRSTA, and if STOP is detected, it will enter IDLE.

Figure 25 Arbitration Timing



14.5.7 Broadcast call addressing

The broadcast call addressing function can be used to address all devices connected to the I2C bus. On the addressing frame, the master can activate the broadcast call addressing function by writing 0x00 to the ADDR in the MADDR register and setting the R/W bit to 0.

The device can support broadcast call addressing function by setting the corresponding enable control bit CTRL[GCEN] to 1. If the GCEN bit has been set to 1 to support broadcast call addressing function, the ACK bit in the CTRL register shall also be set to 1. When the device receives an address frame with a value of 0x00, an acknowledgement signal will be returned. When this condition occurs, the broadcast call flag bit GCS will be set to 1, but the ADRS flag bit will not be set.

14.5.8 Bus error

If an unexpected START or STOP condition occurs while data is being transmitted on the I2C bus and the START or STOP condition is not after the ACK bit, it will be considered as a bus error and data transmission will be aborted. When a bus error event occurs, the corresponding bus error flag bit BUSERR in the SR register will be set to 1, and both the SDA and SCL lines will be released. The I2C module enters an idle state.

14.5.9 Overflow/underflow error

When NOSTR=1 and the following conditions are met, overflow or underflow errors will be detected in slave mode:

- In the receiving process, when a new byte is received but the RXFIFO bit is full, the register has not been read. The received new byte is lost, and NACK is automatically sent to respond to the new byte.

- When a new byte should be sent in the transmission process but TXFIFO is empty, 0xFF will be sent.

When an overflow or underflow error is detected, the OVRS flag in the SR register will be set to 1. If the OVRIE bit is set to 1 in the IEN register, an interrupt will also be generated.

14.5.10 Stretching SCL

Slave mode:

- When NOSTR=0:

(1) Receive the addr+R/W bit, addrmatch flag stretches SCL, waiting for software processing to clear addrmatch flag and clear stretching; the stretching occurs before the ACK data is sent, namely between 8~9 data.

(2) When receiving data, if the RXFIFO is full or the receive data register is full and ACK is sent, SCL will be stretched. When the data is read away, the stretching will be automatically cleared, and the stretching occurs after the ACK data is sent.

(3) When sending data, if TXFIFO is empty or the transmit data register is empty and ACK is received, SCL will be stretched. When FIFO data is written, the stretching will be released, and the stretching occurs after the ACK data is sent.

- When NOSTR=1:

(1) Stretching will not occur in the above situation 1.

(2) If the RXFIFO is full in the above situation 2, Overwrite will occur and the OVRS flag will be pulled up.

(3) If the TXFIFO is empty in the above situation 3, an Overread will occur and the OVRS flag will be pulled up.

Master mode:

(1) The master receives NACK, stretches the clock, waits for software processing, and releases when the NACK flag is cleared.

(2) When the master is transmitting data, if TXFIFO is empty, stretch the clock and wait for software processing; it will be released when data is written to TXFIFO.

(3) When the master is receiving data, if RXFIFO is full, stretch the clock and wait for software processing; it will be released when RXFIFO is read.

14.5.11 TIMEOUT

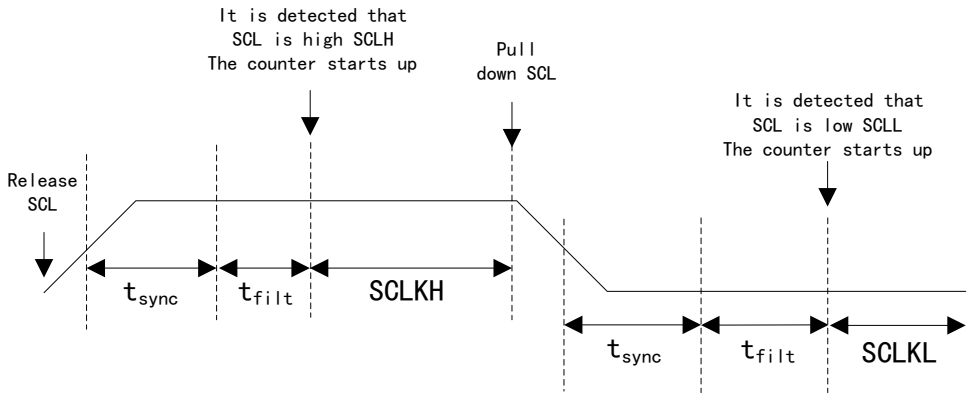
When the low or high-level duration of SCL exceeds the value configured in the

TIMEOUT register during data transmission, a timeout will occur and the TOF bit of the SR register will be set. When the TOFIE bit of the IEN register is set to high, an interrupt will occur. When a timeout occurs, the state machine will jump to IDLE and the bus will be released at the same time.

14.5.12 Clock generation

In master mode, clock generation is related to t_{sync} and t_{filt}, SCLKH, and SCLKL.

Figure 26 clock Generation



T=t_{sync}+t_{filt}+（SCLKH+1）*pclk+（SCLKL+1）*pclk+t_{sync}+t_{filt}

SCL=$\frac{1}{T}$

t_{sync}= 2*pclk

t_{filt}= CTRL[FILT]*plck

SCLKH=SCLC[SCLH]

SCLKL=SCLC[SCLL]

14.6 Register address mapping

Table 28 I2C Register Address Mapping

Register name	Description	Offset address
CTRL	Control register	0x00
SADDR	Slave device address register	0x04
MADDR	Master device address register	0x08
SCLC	Clock configuration register	0x0C
TXDATA	Transmit data FIFO register	0x10
RXDATA	Receive data FIFO register	0x14
TMO	Timeout register	0x18

Register name	Description	Offset address
IEN	Interrupt enable register	0x1C
SR	Status register	0x20
SRC	Status clear register	0x24

14.7 Register functional description

14.7.1 Control register (CTRL)

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	EN	R/W	I2C Enable 0: Disable 1: Enable
1	FFC	W1R0	FIFO Clear 0: Not clear FIFO 1: Clear FIFO Only valid for TXFIFO, can be used to quickly clear TXFIFO
2	GCEN	R/W	General Call Enable 0: Disable 1: Enable Broadcast address 0x00
3	ACK	R/W	Acknowledge 0: Transmit NACK 1: Transmit ACK
4	NOSTR	R/W	No Stretch 0: Enable clock stretching 1: Disable clock stretching Can prevent overload and underload Note: Only valid in slave mode
5	STOP	R/W	STOP 0: No STOP generated 1: Generate STOP after the current data Byte has been sent
6	AUTOEND	R/W	Auto End 0: Not end automatically 1: Automatically send STOP after ACK has been sent and received Note: Valid when sending data in master mode
7	TOEN	R/W	Timeout Enable 0: Disable 1: Enable
9:8	FILT	R/W	Filter 00: bypass 01: 1 pclk 10: 2 pclk

Field	Name	R/W	Description
			11: 3 pclk Filter width (affecting the frequency in master mode)
10	START	R/W	START 0: Not transmit START 1: Transmit START Note: After this bit is configured to 1, START will be sent when the bus is idle. Enter the master mode. In the master mode, configuring this bit will enter transmitting RESTART, and after START is sent, the hardware will automatically clear it to zero
31:11	Reserved		

Note: W1R0 indicates writing 1 to clear, and reading as 0.

14.7.2 Slave device address register (SADDR)

Offset address: 0x04

Reset value: 0x0000 0055

Field	Name	R/W	Description
6:0	SADDR	R/W	Slave Address Address when serving as a slave
31:7	Reserved		

14.7.3 Master device address register (MADDR)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	RD_WR	R/W	Read Write 0: Write data to the slave 1: Read data from the slave
7:1	ADDR	R/W	Address
31:8	Reserved		

14.7.4 Clock configuration register (SCLC)

Offset address: 0x0C

Reset value: 0x0000 FFFF

Field	Name	R/W	Description
7:0	SCLL	R/W	SCL Low Period
15:8	SCLH	R/W	SCL High Period
31:16	Reserved		

Note: I2C main frequency in master mode:

$$\mathrm{CLK} = \frac{pclk}{((\mathrm{SCLH}+1)+\mathrm{CTRL[FILT]}+2+(\mathrm{SCLL}+1)+\mathrm{CTRL[FILT]}+2)}$$

14.7.5 Transmit data FIFO register (TXDATA)

Offset address: 0x10

Reset value: 0x0000 00FF

Field	Name	R/W	Description
7:0	TXDATA	W	Transmit Data FIFO size: 8x8
31:16	Reserved		

14.7.6 Receive data FIFO register (RXDATA)

Offset address: 0x14

Reset value: 0x0000 00FF

Field	Name	R/W	Description
7:0	RXDATA	W	Receive Data FIFO size: 8x8
31:16	Reserved		

14.7.7 Timeout register (TIMEOUT)

Offset address: 0x18

Reset value: 0x00FF FFFF

Field	Name	R/W	Description
23:0	TIMEOUT	R/W	Timeout When CTRL[TOEN] is enabled and the low or high level time exceeds (TIMEOUT+1)*pclk, TIMEOUT will occur
31:24	Reserved		

14.7.8 Interrupt enable register (IEN)

Offset address: 0x1C

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	STAIE	R/W	START Interrupt Enable 0: Disable 1: Enable
1	STOPIE	R/W	STOP Interrupt Enable 0: Disable 1: Enable
2	ADRSIE	R/W	Address Status Interrupt Enable 0: Disable 1: Enable
3	GCSIE	R/W	General Call Status Interrupt Enable 0: Disable 1: Enable
4	ARBLIE	R/W	Arbitration Lost Interrupt Enable 0: Disable 1: Enable

Field	Name	R/W	Description
5	NACKIE	R/W	NACK Interrupt Enable 0: Disable 1: Enable
6	TOFIE	R/W	Timeout Flag Interrupt Enable 0: Disable 1: Enable
7	BUSERRIE	R/W	Bus Error Interrupt Enable 0: Disable 1: Enable
8	OVRIE	R/W	Overflow Interrupt Enable 0: Disable 1: Enable
9	RXFEIE	R/W	RX FIFO Empty Interrupt Enable 0: Disable 1: Enable
10	RXFHIE	R/W	RX FIFO Half Empty Interrupt Enable 0: Disable 1: Enable
11	RXFFIE	R/W	RX FIFO Full Interrupt Enable 0: Disable 1: Enable
12	TXFEIE	R/W	TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
13	TXFHIE	R/W	TX FIFO Half Empty Interrupt Enable 0: Disable 1: Enable
14	TXFFIE	R/W	TX FIFO Full Interrupt Enable 0: Disable 1: Enable
31:15	Reserved		

14.7.9 State register (SR)

Offset address: 0x20

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	STA	R	START condition sending flag (START) 0: No START 1: START is sent/received START is sent in master mode START is received in slave mode
1	STOP	R	STOP Valid in slave mode
2	ADRS	R	Address Status

Field	Name	R/W	Description
			In master mode, it represents the completion of address sending In slave mode, it represents that the address matching is addressed
3	GCS	R	General Call Status
4	ARBLOS	R	Arbitration Lost
5	RXNACK	R	Receive NACK
6	TOF	R	Timeout Flag
7	BUSERR	R	Bus Error Inappropriate timing of START or STOP was detected
8	OVRS	R	Overflow Status The transmit FIFO is empty and continues to transmit data The receive FIFO is full and continues to receive data Valid in slave mode
9	RXFE	R	Receive FIFO Empty
10	RXFH	R	Receive FIFO Half Full When the received data is greater than half, it is set to 1
11	RXFF	R	Receive FIFO Full
12	TXFE	R	Transmit FIFO Empty
13	TXFH	R	Transmit FIFO Half Full When the remaining space of the transmit FIFO is greater than half, it is set to 1
14	TXFF	R	Transmit FIFO Full
15	MSF	R	Master Slave Flag 0: Slave mode 1: Master mode
16	RD_WR	R	Read Write 0: Write (Slave mode: receive Master data) 1: Read (Slave mode: send data to Master) Valid in slave mode
17	BUSY	R	Bus Busy
31:18	Reserved		

14.7.10 State clear register (SRC)

Offset address: 0x24

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	STASC	W1R0	START State Clear
1	STOPSC	W1R0	STOP State Clear

Field	Name	R/W	Description
2	ADRSSC	W1R0	Address State Clear
3	GCSSC	W1R0	General Call State Clear
4	ARBLSC	W1R0	Arbitration Lost State Clear
5	NACKSC	W1R0	NACK State Clear
6	TOFSC	W1R0	Timeout State Clear
7	BUSERRSC	W1R0	Bus Error State Clear
8	OVRSC	W1R0	Overflow State Clear
31:9	Reserved		

Note: W1R0 indicates writing 1 to clear, and reading as 0.

15 Single-Wire Communication Interface (HSC)

15.1 Full Name and Abbreviation Description of Terms

Table 29 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
High Single-Wire Communication	HSC

15.2 Introduction

HSC is a bidirectional communication interface, which uses a single wire, and an open-drain structure. The HSC pins need to be connected to a pull-up resistor. The HSC interface can send a command to the slave of the HSC protocol. This command can directly instruct the slave to receive the next 8-bit/16 bit data (write command), or retrieve 8-bit/16-bit data from a specific register and output it to the HSC communication line (read command).

In a string of data, the address data is first transmitted. Similar to other protocols, the address data consists of 7 bits, plus one-bit read/write command, forming an 8-bit data. The 8-bit/16-bit data (HSC8/HSC16) is next transmitted.

15.3 Main characteristics

(1) Support master/slave mode

(2) Support 8-bit/16-bit data format transmission

(3) Only a single line is needed

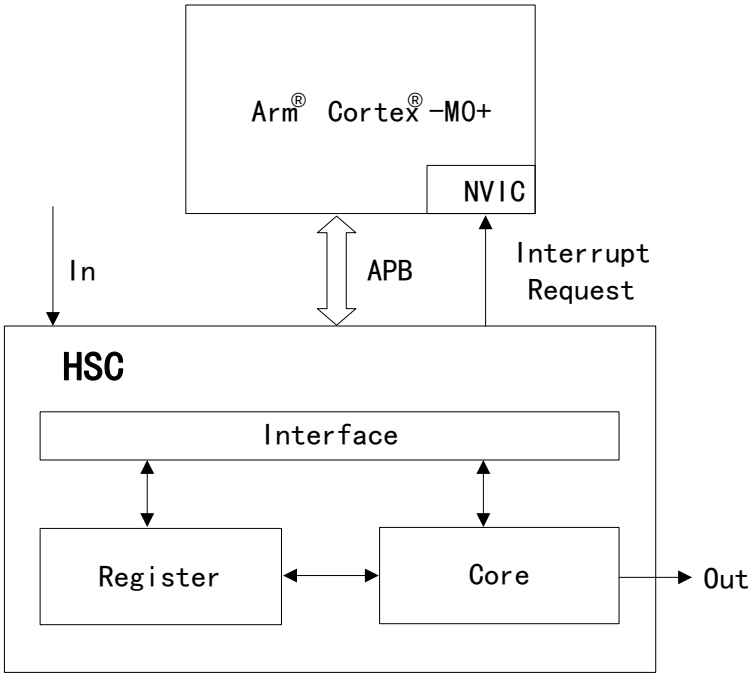
(4) Support error frame detection

(5) Support interrupt of data transmission completion

(6) Support programmable t_{HW1} startup detection

15.4 Structure block diagram

Figure 27 Structure Block Diagram

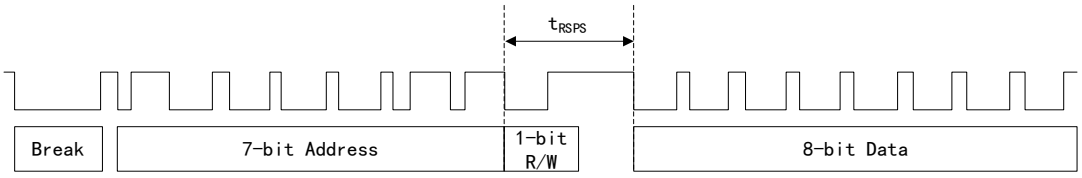


15.5 Functional description

When the HSC bus is in an idle state, the HSC signal pulls the HSC to a high level through the external pull-up resistor.

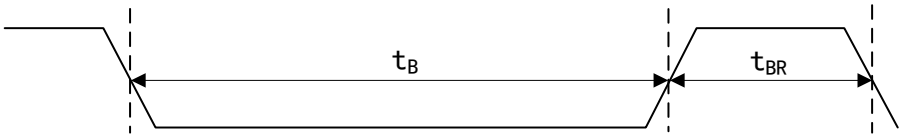
Transmission of data 0 and 1 through HSC communication is controlled by the time of high and low levels. The data frame format includes a Break bit, a 7-bit address, and an R/W identification bit, followed by the transmitted data bit. Below is a typical data transmission timing diagram of HSC.

Figure 28 HSC Data Transmission Timing Diagram



As shown in the figure below, if the HSC communication line is pulled down for more than 190us, i.e. t_B time, the HSC communication will be reset. Therefore, if the master does not receive the expected data from the slave or wants to start a new communication by the end of this communication, it can reset the communication by sending a Break, and start the next communication after a minimum communication recovery time of 40us after the Break.

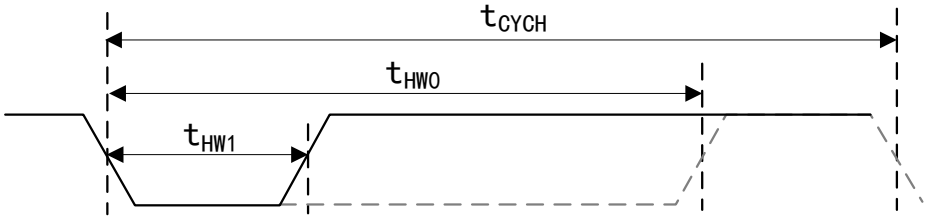
Figure 29 HSC Break and Break Recovery Timing Diagram



Parameters of t_B and t_{BR} in the above figure:

- t_B: Break time
- t_{BR}: Break recovery time

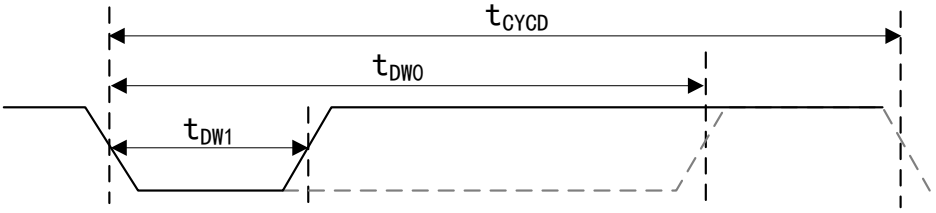
Figure 30 HSC Host Transmission 0 or 1 Timing



Parameters of t_{HW1}, t_{HW0}, and t_{CYCH} in the above figure:

- t_{HW1}: The time when the master writes 1 after the master drives HSC
- t_{HW0}: The time when the master writes 0 after the master drives HSC
- t_{CYCH}: The cycle time from the master to the device after the master drives HSC

Figure 31 HSC Slave Transmission 0 or 1 Timing



Parameters of t_{DW1}, t_{DW0}, and t_{CYCD} in the above figure:

- t_{DW1}: The time when the device writes 1 after the device drives HSC
- t_{DW0}: The time when the device writes 0 after the device drives HSC
- t_{CYCD}: The cycle time from the device to the master after the device drives HSC

15.6 Register address mapping

Table 30 HSC Register Address Mapping

Register name	Description	Offset address
CTRL	Control register	0x00
HCMD	Command register	0x04
HAD	Data register	0x08

Register name	Description	Offset address
IEN	Interrupt enable register	0x0C
SR	Status register	0x10
SRC	Status clear register	0x14

15.7 Register functional description

15.7.1 Control register (CTRL)

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	EN	R/W	HSC Enable 0: Disable 1: Enable
1	START	W1R0	Start 0: Not transmit 1: Start transmission or restart Note: It will be automatically cleared to zero after writing 1. Master mode: Used to start transmission and restart, but unable to restart when BRKEN=1. Slave mode: After receiving the address, if it is a read slave, it is used to start sending data.
2	MODE	R/W	Mode 0: Slave 1: Master
4:3	THW1	R/W	t_{HW1} Setting 00: 0.5us~50us (1us~50us 1M system clock) 01: 17us~50us 10：32us~50us 11：0.5us~50us Note: Slave mode is valid. Determine whether communication will be initiated. When the low level is less than the selected value, communication will not be initiated.
5	BITS	R/W	Bits Protocol Select 0: 8-bit data protocol 1: 16-bit data protocol
6	BRKEN	R/W	Break Enable 0: Transmit break 1: Not transmit break Note: Master mode is valid.
9:7	CLKSEL	R/W	Clock Select 0: System clock 4MHz 1: System clock 2MHz 2: System clock 8MHz 3: System clock 16MHz

Field	Name	R/W	Description
			4: System clock 1MHz RFU: System clock 4MHz
10	TOEN	R/W	Timeout Enable 0: Disable 1: Enable If Timeout is enabled, it will occur when the low level exceeds 2.2s or the period of one bit exceeds 2.2s
31:11	Reserved		

Note: W1R0 indicates writing 1 to clear, and reading as 0.

15.7.2 Command register (HCMD)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
6:0	MSADDR	R/W	Master Slave Address As the address sent by the master, as the address received by the slave
7	MRW	R/W	Master Read Write 0: Read data (read data from the slave in master mode, and send data from the slave to the master in slave mode) 1: Write data (write data to the slave in master mode, and receive data sent by the master in slave mode)
31:8	Reserved		

15.7.3 Data register (HDA)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	HDATA0	R/W	HSC Data0
15:8	HDATA1	R/W	HSC Data1
31:16	Reserved		

15.7.4 Interrupt enable register (IEN)

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	BRKEN	R/W	Break Enable 0: Disable 1: Enable
1	CMDEN	R/W	Command Enable 0: Disable 1: Enable
2	DATAEN	R/W	Data Enable

Field	Name	R/W	Description
			0: Disable 1: Enable
3	FREN	R/W	Frame Enable 0: Disable 1: Enable
4	TOEN	R/W	Timeout Enable 0: Disable 1: Enable
31:5	Reserved		

15.7.5 State register (SR)

Offset address: 0x10

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	BRKS	R	Break Status 1: Break is completed 0: Break is not completed
1	CMDS	R	Command Status 1: Command transmission is completed 0: No command transmission is completed
2	DATAS	R	Data Status 1: Data transmission is completed 0: No data transmission is completed
3	FRS	R	Frame Status 1: A frame error occurred 0: No frame error transmitted
4	TIMEOUT	R	Timeout 1: Timed out 0: Not timed out Note: Timeout will occur when the low-level time is greater than 2.2s or the time of a data bit exceeds 2.2s
5	BUSY	R	Busy 1: Busy 0: Idle Note: It will be automatically cleared to zero after data transmission is completed
31:6	Reserved		

15.7.6 State clear register (SRC)

Offset address: 0x14

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	BRKSC	W1R0	Break Status Clear
1	CMDSC	W1R0	Command Status Clear

Field	Name	R/W	Description
2	DATASC	W1R0	Data Status Clear
3	FRSC	W1R0	Frame Status Clear
4	TOSC	W1R0	Timeout Status Clear
31:5	Reserved		

Note: W1R0 indicates writing 1 to clear, and reading as 0.

16 Universal Asynchronous Receiver/Transmitter (UART)

16.1 Full Name and Abbreviation Description of Terms

Table 31 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
First-In First-Out	FIFO
Universal Asynchronous Receiver Transmitter	UART
Most Significant Bit	MSB
Least Significant Bit	LSB

16.2 Introduction

UART is a serial communication device that can flexibly conduct full-duplex and half-duplex data exchange with external devices. 1 UART communication interface is embedded, and it supports full-duplex independent receiving and transmitting channels.

16.3 Main characteristics

(1) Full-duplex communication

(2) Configurable baud rate

(3) Support 8-bit data width transmission

(4) Configurable parity bit enable

(5) Configurable stop bit

(6) Independent transmitting and receiving configuration

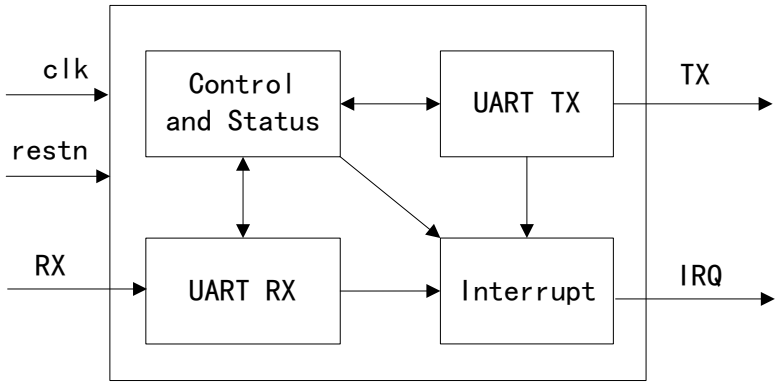
(7) Transmission error detection

(8) Programmable data transmission sequence, supporting shifting MSB or LSB first

(9) Built-in 4-byte transmit and receive buffer

16.4 Structure block diagram

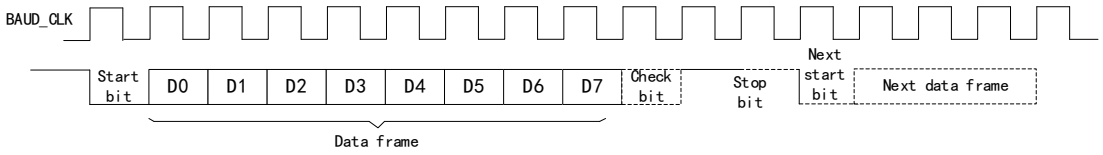
Figure 32 Structure Block Diagram



16.5 Functional description

As shown in the figure below, the data transmitted by UART is organized into data packets in the format of 1 start bit, 1 data frame, 1 optional parity bit, and 1 or 2 stop bits.

Figure 33 UART Communication Timing



The transmission line usually remains at a high level when not transmitting data. The start bit of a low level in one transmission cycle indicates the start of data transmission, followed by the transmitting data frame, which contains the actual transmitted data. The sequence MSB/LSB of data frame transmission is configurable, the data frame is followed by optional parity bit, which is used to check if the transmitted data is correct, and finally a high-level stop bit is sent for 1 or 2 cycles to indicate the end of transmission.

16.6 Register address mapping

Table 32 UART Register Address Mapping

Register name	Description	Offset address
UART_CR	Control register	0x00
UART_TDR	Transmit data register	0x04
UART_RDR	Receive data register	0x08
UART_IER	Interrupt enable register	0x0C
UART_SR	Status register	0x10

Register name	Description	Offset address
UART_SCR	Status clear register	0x14
UART_BDR	Baud rate configuration register	0x18

16.7 Register functional description

16.7.1 Control register (UART_CR)

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	TXE	R/W	Transmit Enable 0: Disable 1: Enable
1	RXE	R/W	Receive Enable 0: Disable 1: Enable
2	STOPBIT	R/W	Stop Bit 0: Configure 1-bit stop bit 10: Configure 2-bit stop bit
3	PARITYE	R/W	Parity Enable 0: Disable 1: Enable
4	PARITYSEL	R/W	Parity Select 0: Odd parity check 1: Even parity check Note: This bit takes effect on the premise that parity check is enabled
5	TXSEQSEL	R/W	Transmit Sequence Select 0: LSB first 1: MSB first
6	ABE	R/W	Auto Baudrate Enable 0: Disable 1: Enable
31:7	Reserved		

16.7.2 Transmit data register (UART_TDR)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	TXDATA	R/W	Transmit Data 8-bit data to be transmitted
31:8	Reserved		

16.7.3 Receive data register (UART_RDR)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	RXDATA	R	Receive Data Received 8-bit data
31:8	Reserved		

16.7.4 Interrupt enable register (UART_IER)

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	TXIE	R/W	Transmit Interrupt Enable 0: Disable 1: Enable
1	RXIE	R/W	Receive Interrupt Enable 0: Disable 1: Enable
2	TXOEIE	R/W	TX Overflow Error Interrupt Enable 0: Disable 1: Enable
3	RXOEIE	R/W	RX Overflow Error Interrupt Enable 0: Disable 1: Enable
4	PEIE	R/W	Parity Error Interrupt Enable 0: Disable 1: Enable
5	FEIE	R/W	Frame interrupt Enable 0: Disable 1: Enable
6	TXBUFFUIE	R/W	TX Buffer Full Interrupt Enable 0: Disable 1: Enable
7	RXBUFFUIE	R/W	RX Buffer Full Interrupt Enable 0: Disable 1: Enable
8	TXBUFEMIE	R/W	TX Buffer Empty Interrupt Enable 0: Disable 1: Enable
9	RXBUFEMIE	R/W	RX Buffer Empty Interrupt Enable 0: Disable 1: Enable
10	TXBUFHAFUIE	R/W	TX Buffer Half Full Interrupt Enable 0: Disable 1: Enable
11	RXBUFHAFUIE	R/W	RX Buffer Half Full Interrupt Enable 0: Disable 1: Enable

Field	Name	R/W	Description
12	ABCIE	R/W	Auto Baudrate Complete Interrupt Enable 0: Disable 1: Enable
13	ABEIE	R/W	Auto Baudrate Error Interrupt Enable 0: Disable 1: Enable
31:14	Reserved		

16.7.5 State register (UART_SR)

Offset address: 0x10

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	TXCF	R/W	Transmit Complete Flag 0: Transmission is not completed 1: Transmission is completed
1	RXCF	R	Receive Complete Flag 0: Receiving is not completed 1: Receiving is completed
2	TXOERRF	R	TX Overflow Error Flag If new transmitted data is written when the transmit buffer data has not been loaded into the internal shift register, an overflow error will occur, and the transmit buffer will be overwritten by the newly written data 0: Transmitting data without overflow error 1: Transmitting data overflow error
3	RXOERRF	R	RX Overflow Error Flag If new data is received when the receive buffer data has not been read out, an overflow error will occur, and the receive buffer will be overwritten by the new data 0: Receiving data without overflow error 1: Receiving data overflow error
4	PERRF	R	Parity Error Flag 0: The parity check of the received data is correct 1: The parity check of the received data is wrong
5	FERRF	R	Frame Error Flag 0: The received data stop bit meets expectation 1: The received data stop bit is incorrect
6	TXBUFFULL	R	TX Buffer Full It will be automatically cleared to 0 by hardware after the transmitted data is sent to the shift register 0: The transmit buffer is not full, and the transmitted data can be written at this time 1: The transmit buffer has been full
7	RXBUFFULL	R	RX Buffer Full It will be automatically cleared to 0 after the received data is read out 0: The receive buffer is not full

Field	Name	R/W	Description
			1: The receive buffer is full, and the data is not read out at this time
8	TXBUFEMP	R	TX Buffer Empty 0: The transmit buffer is not empty 1: The transmit buffer is empty
9	RXBUFEMP	R	RX Buffer Empty 0: The receive buffer is not empty 1: The receive buffer is empty
10	TXBUFHAFUL	R	TX Buffer Half Full 0: Non-half data is remaining 1: Half data is remaining
11	RXBUFHAFUL	R	RX Buffer Half Full 0: Non-half data is remaining 1: Half data is remaining
12	TXBSY	R	Transmit Busy When TX transmission starts, it will be set to 1. After transmission is completed, it will be automatically cleared to 0 by hardware 0: In idle state 1: Being transmitted
13	RXBSY	R	Receive Busy It is valid when RX successfully detects the start bit, and will be automatically cleared to 0 by hardware when the receiving ends 0: In idle state 1: In the process of receiving
14	ABCF	R	Auto Baudrate Complete Flag 0: Automatic baud rate detection is not completed 1: Automatic baud rate detection is completed
15	ABERR	R	Auto Baudrate Error 0: No automatic baud rate detection error 1: Automatic baud rate detection error (baud rate exceeding the range of 16~65535 or receiving data error)
31:16	Reserved		

16.7.6 State clear register (UART_SCR)

Offset address: 0x14

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	CTXC	W	Clear TX Complete
1	CRXC	W	Clear RX Complete
2	CTXOERR	W	Clear TX Overflow Error
3	CRXOERR	W	Clear RX Overflow Error
4	CPERR	W	Clear Parity Error
5	CFERR	W	Clear Frame Error
6	CABC	W	Clear Auto Baudrate Complete

Field	Name	R/W	Description
7	CABERR	W	Clear Auto Baudrate Error
31:8	Reserved		

16.7.7 Baud rate configuration register (UART_BDR)

Offset address: 0x18

Reset value: 0x0000 0023

Field	Name	R/W	Description
15:0	BAUDDIV	R/W	Baudrate Division Baud rate=UART_PCLK/BAUDDIV (the default value is calculated based on pclk of 4MHz and baud rate of 115200bps)
31:16	Reserved		

17 Analog-to-Digital Converter (ADC)

17.1 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Analog to Digital Converter	ADC
Injected	INJ
Sample	SMP
Programmable Gain Amplifier	PGA
Multiplexer	MUX

17.2 C-ADC converter

17.2.1 Introduction

C-ADC is a 16-bit Σ-Δ analog-to-digital converter for sampling the current, and the reference voltage V_{ref} is generated from V_{DD}.

17.2.2 Main characteristics

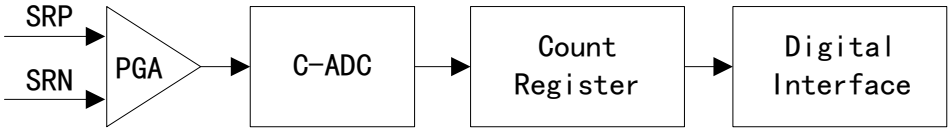
(1) C-ADC is differential input

(2) Automatic zero calibration

(3) C-ADC interrupt can wake up the system in idle mode

17.2.3 Structure block diagram

Figure 34 Structure Block Diagram



For C-ADC, C-ADC Data= (V_{SRP}–V_{SRN}) / (V_{REF}+–V_{REF}-) × 32768

If the conversion result of negative differential full input is 0x8000, zero differential input is converted; if the result is 0x0000, the conversion result of positive differential full input is 0x7FFF.

17.2.4 Functional description

The CADCEN signal controls the C-ADC enable, and after the RSTN signal is released, the C-ADC reset is completed, the conversion starts, and the SP_DONE indicates the end of conversion. After the conversion is completed, update the C-ADC data register and generate an interrupt (if the C-ADC interrupt is allowed).

C-ADC converts the SRP/SRN input signal and places the conversion result in the C-ADC register.

17.2.5 Register address mapping

Table 33 C-ADC Register Address Mapping

Register name	Description	Offset address
CTRL	Control register	0x00
IEN	Interrupt enable register	0x10
SR	Status register	0x14
SCR	Status clear register	0x18
SDATA	Source data register	0x1C

17.2.6 Register functional description

17.2.6.1 Control register (CTRL)

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	EN	R/W	ADC Enable 0: Disable 1: Enable
1	CHP_EN	R/W	Chopper Enable 0: Disable 1: Enable
2	CHPDLY_SEL_C	R/W	Chopper Delay Select
4:3	OSR_SEL	R/W	Over Sample Rate Select 00: 128 01: 256 10: 512 11: 1024
5	CADC_CLK_BOOST	R/W	C-ADC Clock Boost Enable 0: Disable 1: Enable
31:6	Reserved		

Note: When reading the CTRL register of the C-ADC, ensure that the AFECLOCKEN bit in the SYSCCTRL_ANACR register is set to 1. Otherwise, it may cause the system to become unresponsive.

17.2.6.2 Interrupt enable register (IEN)

Offset address: 0x10

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	SPDIEN	R/W	Sample Done Interrupt Enable 0: Disable 1: Enable

Field	Name	R/W	Description
31:1	Reserved		

17.2.6.3 State register (SR)

Offset address: 0x14

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	SP_DONE	R	Sample Done 0: No data is sampled 1: Data sampling is completed
31:1	Reserved		

17.2.6.4 State clear register (SCR)

Offset address: 0x18

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	SPDC	W1R0	Sample Done Clear It can be cleared by writing 1, and will be automatically cleared to 0 by hardware after writing 1
31:1	Reserved		

Note: W1R0 indicates writing 1 to clear, and reading as 0.

17.2.6.5 Source data register (SDATA)

Offset address: 0x1C

Reset value: 0x0000 0000

Field	Name	R/W	Description
19:0	DATA	R	Source ADC Data
31:20	Reserved		

17.3 V-ADC converter

17.3.1 Introduction

V-ADC is a 16-bit Σ-Δ analog-to-digital converter for voltage sampling. The reference voltage V_{ref} is generated by V_{DD}, and it provides 2-bit ADC input channel selection.

17.3.2 Main characteristics

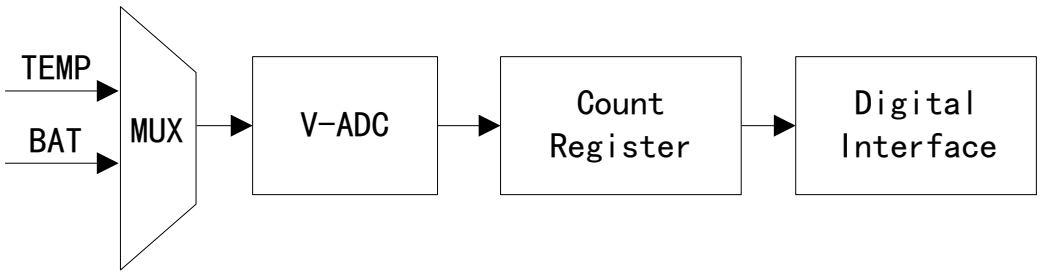
(1) V-ADC is 2 single-ended inputs

(2) Automatic zero calibration

(3) V-ADC interrupt can wake up the system in idle mode

17.3.3 Structure block diagram

Figure 35 Structure Block Diagram



17.3.4 Functional description

The VADCEN signal controls the V-ADC enable, and after the RSTN signal is released, the V-ADC reset is completed, the conversion starts, and the SP_DONE indicates the end of conversion. After the conversion is completed, update the V-ADC data register and generate an interrupt (if the V-ADC interrupt is allowed).

V-ADC provides automatic conversion function, which can set some channels to automatically switch, and automatically complete the required delay. After all data tests are completed, an interrupt will be generated.

17.3.5 Register address mapping

Table 34 V-ADC Register Address Mapping

Register name	Description	Offset address
CTRL	Control register	0x00
IEN	Interrupt enable register	0x10
SR	Status register	0x14
SCR	Status clear register	0x18
SDATA	Source data register	0x1C

17.3.6 Register functional description

17.3.6.1 Control register (CTRL)

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	EN	R/W	ADC Enable 0: Disable 1: Enable
1	CHP_EN	R/W	Enable Chopper port 0: Disable 1: Enable
2	CHPDLY_SEL_C	R/W	Chopper delay selection port
4:3	OSR_SEL	R/W	Over Sample Rate Select 00: 128 01: 256 10: 512 11: 1024
31:5	Reserved		

Note: When reading the CTRL register of the C-ADC, ensure that the AFECLOCKEN bit in the SYSCCTRL_ANACR register is set to 1. Otherwise, it may cause the system to become unresponsive.

17.3.6.2 Interrupt enable register (IEN)

Offset address: 0x10

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	SPDIEN	R/W	Sample Done Interrupt Enable 0: Disable sampling interrupt 1: Enable sampling interrupt
31:1	Reserved		

17.3.6.3 State register (SR)

Offset address: 0x14

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	SP_DONE	R	Sample Done 0: No data is sampled 1: Data sampling is completed
1	VOL_SEL	R	Voltage Select 0: V_{REF} 2.7V 1: V_{REF} 1.8V
31:2	Reserved		

17.3.6.4 State clear register (SCR)

Offset address: 0x18

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	SPDC	W1R0	Sample Done Clear It can be cleared by writing 1, and will be automatically cleared to 0 by hardware after writing 1
31:1	Reserved		

Note: W1R0 indicates writing 1 to clear, and reading as 0.

17.3.6.5 Source data register (SDATA)

Offset address: 0x1C

Reset value: 0x0000 0000

Field	Name	R/W	Description
19:0	DATA	R	Source ADC Data
31:20	Reserved		

18 Hash Algorithm (SHA256)

18.1 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Secure Hash Algorithm	SHA
Hash-based Message Authentication Code	HMAC
Message Authentication Code	MAC

18.2 Introduction

The SHA256 algorithm is a classic hash algorithm, which can convert data of any length into data of fixed length. This algorithm has strong collision resistance and is irreversible. The SHA256 algorithm can be applied in such fields as data signature, data consistency, privacy protection, and user password protection.

18.3 Main characteristics

(1) Support up to 256-bit message input, with configurable length. The key length is fixed at 256 bits

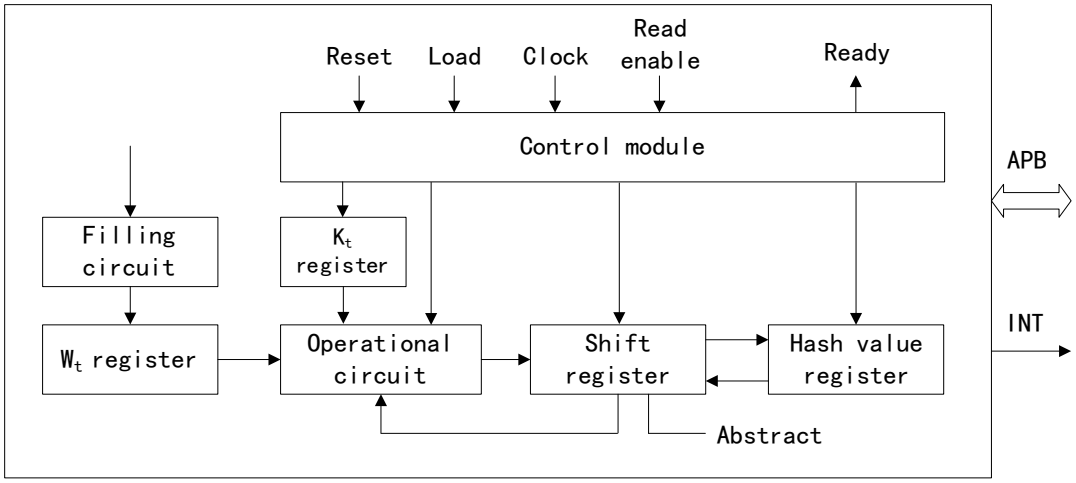
(2) Support independent 512-bit input SHA256 operation mode

(3) Support both general and dedicated working modes

(4) Configurable operation completion interrupt

18.4 Structure block diagram

Figure 36 Structure Block Diagram



18.5 Functional description

The hash message authentication code (HMAC) is a message authentication code (MAC) generated through a special calculation method of using a cryptographic hash function combined with an encryption key. The HMAC-SHA256 algorithm, i.e. HMAC algorithm using SHA256 to generate hash values.

The chip can use HMAC-SHA25 to implement security authentication, and it needs about 256 pclk periods (assuming pclk is 4MHz, about 64 us) to complete one operation process and obtain the authentication result. It also supports switching to an independent 512-bit input SHA256 operation mode. The software can use this operation mode to perform SHA256 operations of any length, and it needs about 64 pclk periods (assuming pclk is 4MHz, about 16 us) to complete one operation process and obtain the authentication result.

18.6 Register address mapping

Table 35 SHA256 Register Address Mapping

Register name	Description	Offset address
HMAC_CR	Control register	0x00
HMAC_KEY7R	Key 7 register	0x04
HMAC_KEY6R	Key 6 register	0x08
HMAC_KEY5R	Key 5 register	0x0C
HMAC_KEY4R	Key 4 register	0x10
HMAC_KEY3R	Key 3 register	0x14
HMAC_KEY2R	Key 2 register	0x18
HMAC_KEY1R	Key 1 register	0x1C
HMAC_KEY0R	Key 0 register	0x20
HMAC_MSG7R	Message 7 register	0x24
HMAC_MSG6R	Message 6 register	0x28
HMAC_MSG5R	Message 5 register	0x2C
HMAC_MSG4R	Message 4 register	0x30
HMAC_MSG3R	Message 3 register	0x34
HMAC_MSG2R	Message 2 register	0x38
HMAC_MSG1R	Message 1 register	0x3C
HMAC_MSG0R	Message 0 register	0x40
HMAC _SR	Status register	0x44

Register name	Description	Offset address
HMAC _SCR	Status clear register	0x48
HMAC_RES7R	Result 7 register	0x4C
HMAC_ RES6R	Result 6 register	0x50
HMAC_ RES5R	Result 5 register	0x54
HMAC_ RES4R	Result 4 register	0x58
HMAC_ RES3R	Result 3 register	0x5C
HMAC_ RES2R	Result 2 register	0x60
HMAC_ RES1R	Result 1 register	0x64
HMAC_ RES0R	Result 0 register	0x68

18.7 Register functional description

18.7.1 Control register (HMAC_CR)

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	HMACE	R/W	HMAC Enable 0: Disable 1: Enable Write operation can be performed on the key, message registers, and result registers only after it is enabled
1	START	R/W	Start HMAC 0: The calculation is not started 1: The calculation is started Set START to start the HMAC operation, and it will be automatically cleared to 0 by hardware after the operation is completed
2	HMACIE	R/W	HMAC Interrupt Enable 0: Disable 1: Enable
3	WKMD	R/W	Work Mode 0: General mode 1: Dedicated mode (reverse the initial value sequence of SHA256 compression function k_i(0~63))
4	OPMD	R/W	Operation Mode 0: Perform HMAC-SHA256 operation 1: Perform SHA256 operation on independent 51-bit input
13:5	MSGLEN	R/W	Message Length 9’h100: 256 bits 9’hFF: 255 bits … 9’h1: 1 bit

Field	Name	R/W	Description
31:14	Reserved		

18.7.2 Key 7 register (HMAC_KEY7R)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	KEY7R	R/W	HMAC key 7 register (Key7) In HMAC-SHA256 operation mode, the value written to this register is the key [255:224]; In SHA256 operation mode, the value written to this register corresponds to the message [511:480]

18.7.3 Key 6 register (HMAC_KEY6R)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	KEY6R	R/W	HMAC key 6 register (Key6) In HMAC-SHA256 operation mode, the value written to this register is the key [223:192]; In SHA256 operation mode, the value written to this register corresponds to the message [479:448]

18.7.4 Key 5 register (HMAC_KEY5R)

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	KEY5R	R/W	HMAC key 5 register (Key5) In HMAC-SHA256 operation mode, the value written to this register is the key [191:160]; In SHA256 operation mode, the value written to this register corresponds to the message [447:416]

18.7.5 Key 4 register (HMAC_KEY4R)

Offset address: 0x10

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	KEY4R	R/W	HMAC key 4 register (Key4) In HMAC-SHA256 operation mode, the value written to this register is the key [159:128]; In SHA256 operation mode, the value written to this register corresponds to the message [415:384]

18.7.6 Key 3 register (HMAC_KEY3R)

Offset address: 0x14

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	KEY3R	R/W	HMAC key 3 register (Key3)

Field	Name	R/W	Description
			In HMAC-SHA256 operation mode, the value written to this register is the key [127:96]; In SHA256 operation mode, the value written to this register corresponds to the message [383:352]

18.7.7 Key 2 register (HMAC_KEY2R)

Offset address: 0x18

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	KEY2R	R/W	HMAC key 2 register (Key2) In HMAC-SHA256 operation mode, the value written to this register is the key [95:64]; In SHA256 operation mode, the value written to this register corresponds to the message [351:320]

18.7.8 Key 1 register (HMAC_KEY1R)

Offset address: 0x1C

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	KEY1R	R/W	HMAC key 1 register (Key1) In HMAC-SHA256 operation mode, the value written to this register is the key [63:32]; In SHA256 operation mode, the value written to this register corresponds to the message [319:288]

18.7.9 Key 0 register (HMAC_KEY0R)

Offset address: 0x20

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	KEY0R	R/W	HMAC key 0 register (Key0) In HMAC-SHA256 operation mode, the value written to this register is the key [31:0]; In SHA256 operation mode, the value written to this register corresponds to the message [287:256]

18.7.10 Message 7 register (HMAC_MSG7R)

Offset address: 0x24

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	MSG7R	R/W	HMAC message 7 register (Message7) The value written to this register is message [255:224]

18.7.11 Message 6 register (HMAC_MSG6R)

Offset address: 0x28

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	MSG6R	R/W	HMAC message 6 register (Message6) The value written to this register is message [223:192]

18.7.12 Message 5 register (HMAC_MSG5R)

Offset address: 0x2C

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	MSG5R	R/W	HMAC message 5 register (Message5) The value written to this register is message [191:160]

18.7.13 Message 4 register (HMAC_MSG4R)

Offset address: 0x30

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	MSG4R	R/W	HMAC message 4 register (Message4) The value written to this register is message [159:128]

18.7.14 Message 3 register (HMAC_MSG3R)

Offset address: 0x34

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	MSG3R	R/W	HMAC message 3 register (Message3) The value written to this register is message [127:96]

18.7.15 Message 2 register (HMAC_MSG2R)

Offset address: 0x38

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	MSG2R	R/W	HMAC message 2 register (Message2) The value written to this register is message [95:64]

18.7.16 Message 1 register (HMAC_MSG1R)

Offset address: 0x3C

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	MSG1R	R/W	HMAC message 1 register (Message1) The value written to this register is message [63:32]

18.7.17 Message 0 register (HMAC_MSG0R)

Offset address: 0x40

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	MSG0R	R/W	HMAC message 0 register (Message0) The value written to this register is message [31:0]

18.7.18 Status register (HMAC_SR)

Offset address: 0x44

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	INTF	R	Interrupt Flag

Field	Name	R/W	Description
			0: Operation completion interrupt is not set 1: Operation completion interrupt is set This bit is cleared to 0 by software operation HMAC_SCR/CINFT
1	DONE	R	Done 0: Not completed 1: Completed It is automatically cleared to 0 by hardware when HMAC_CR/START is set
31:2	Reserved		

18.7.19 State clear register (HMAC_SCR)

Offset address: 0x48

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	CINTF	W	Clear Interrupt Flag Clear HMAC_SR/INTF by writing 1
31:1	Reserved		

18.7.20 Result 7 register (HMAC_RES7R)

Offset address: 0x4C

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	RES7R	R/W	HMAC result 7 register (Result7) The read-out value of this register is the operation result [255:224]; It can be written in SHA256 operation mode, and the written value is the Hash initial value [255:224] to be involved in the operation

18.7.21 Result 6 register (HMAC_RES6R)

Offset address: 0x50

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	RES6R	R/W	HMAC result 6 register (Result6) The read-out value of this register is the operation result [223:192]; It can be written in SHA256 operation mode, and the written value is the Hash initial value [223:192] to be involved in the operation

18.7.22 Result 5 register (HMAC_RES5R)

Offset address: 0x54

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	RES5R	R/W	HMAC result 5 register (Result5)

Field	Name	R/W	Description
			The read-out value of this register is the operation result [191:160]; It can be written in SHA256 operation mode, and the written value is the Hash initial value [191:160] to be involved in the operation

18.7.23 Result 4 register (HMAC_RES4R)

Offset address: 0x58

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	RES4R	R/W	HMAC result 4 register (Result4) The read-out value of this register is the operation result [159:128]; It can be written in SHA256 operation mode, and the written value is the Hash initial value [159:128] to be involved in the operation

18.7.24 Result 3 register (HMAC_RES3R)

Offset address: 0x5C

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	RES3R	R/W	HMAC result 3 register (Result3) The read-out value of this register is the operation result [127:96]; It can be written in SHA256 operation mode, and the written value is the Hash initial value [127:96] to be involved in the operation

18.7.25 Result 2 register (HMAC_RES2R)

Offset address: 0x60

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	RES2R	R/W	HMAC result 2 register (Result2) The read-out value of this register is the operation result [95:64]; It can be written in SHA256 operation mode, and the written value is the Hash initial value [95:64] to be involved in the operation

18.7.26 Result 1 register (HMAC_RES1R)

Offset address: 0x64

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	RES1R	R/W	HMAC message 1 register (Result1) The read-out value of this register is the operation result [63:32]; It can be written in SHA256 operation mode, and the written value is the Hash initial value [63:32] to be involved in the operation

18.7.27 Result 0 register (HMAC_RES0R)

Offset address: 0x68

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	RES0R	R/W	HMAC message 0 register (Result0) The value written to this register is the operation result [31:0]; It can be written in SHA256 operation mode, and the written value is the Hash initial value [31:0] to be involved in the operation

19 Revision history

Table 36 Document Revision History

Date	Version	Revision History
February 2025	1.0	New

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8. Scope of Application

The information in this document replaces the information provided in all previous versions of the document.